# CHAPTER 4

# MODELING OF PULSE DENSITY MODULATION CONTROL

## 4.1. SYSTEM DESCRIPTION AND OPERATION

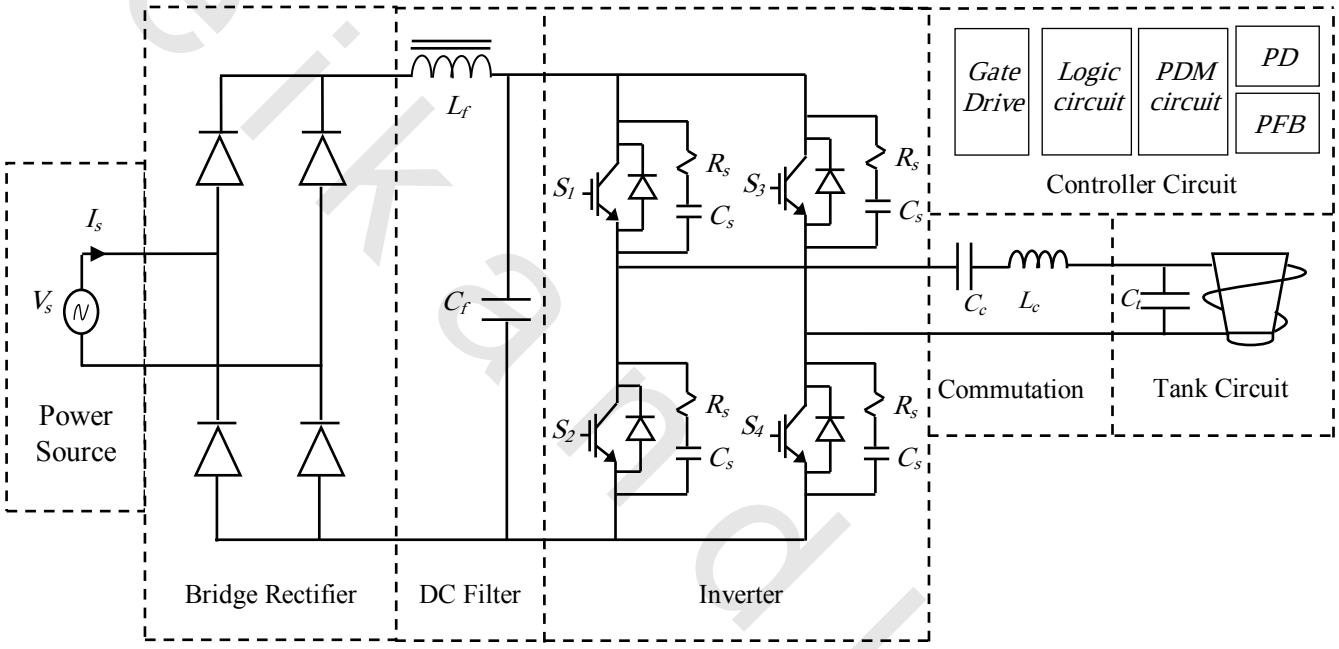



Figure 4.1 Schematic layout of proposed induction heating system.

The typical system configuration of the PDM based induction heating system is shown in Figure 4.1, which comprises the following components:

- Single phase uncontrolled bridge rectifier supplied by a single-phase line frequency (50 Hz) source. It is less complex, less expensive [8], and no need for voltage control circuit, which gives the PDM system an advantage over the load resonant generator;
- Inductive input DC filter or iron core reactor used for smoothing the DC input current for the inverter. The value of the filtering capacitor was selected to minimize the ripples in the DC voltage as possible. The output current of the rectifier can be maintained at a steady value if the inductance of $L_f$ is sufficiently large. The iron core reactor also provides inherent short circuit protection as it restricts the rate of rise of current at a short circuit occurring. The critical inductance is given by [3], [6]:

$$L_f = \frac{R}{6\pi f_i} \qquad \text{Eq. 4.1}$$

Where, $f_i$ is the input source frequency and $R$ is the load resistance;

- A 30 KHz full-bridge series-resonant IGBT inverter, which is modeled and operated at average power of 15 kW. The inverter switches are operated in alternate run and stop modes controlling the pulse width to generate the high frequency alternating current needed to produce a huge eddy current in the work-coil. The run and stops modes are controlled as described in (section 3.5.2.2). The inverter operates at the load resonant frequency allowing zero current switching that increases the inverter efficiency. Each semiconductor is connected with internally anti-parallel freewheeling diode and a parallel *RC* snubber network which improves the performance and protects the device;
- The tank circuit that consists of water-cooled coil that may made to resonate at the resonance frequency by a capacitor placed in parallel with it;
- The power transferred to the load is regulated by a new PDM control system, which forms the main contribution for this research. This is given by the PDM controller blocks shown in Figure 4.1.

## 4.2. MODELING OF THE NEW PDM CONTROLLER

The proposed pulse density modulation control of the resonant inverter is achieved by having three stages feedback control system that combines power feedback (PFB), pulse density modulation control (PDM) and phase angle detection (PD), as shown in Figure 4.1, in order to achieve proper load power regulation and unity power factor.

The proposed output power closed loop controller for series-resonant inverter under PDM technique is shown in Figure 4.2. The inverter instantaneous output current and voltage ($i_{inv}$, $V_{inv}$) are applied to two feedback circuits (PD and PFB).

The concept of PD circuit is shown in Figures 4.3, as it detects the phase difference between the inverter output voltage and current $\Theta_{act}$. Figure 4.3 shows the inverter voltage ($v_{inv}$) and current ($i_{inv}$) signals that are converted from sine to square waves. These square waves are fed to exclusive OR gate (its output is high when its inputs are different) producing $Ph^*$ signal, the later signal is fed to AND gate with the squared voltage signal ($V_{inv\,sq}$) producing a square wave ($Ph_{act}$). The width of the latter pulse represents the phase difference time ($T_{ph}$). The $Ph_{act}$ is fed to AND gate with clock signal with frequency of ($1/t_{clk}$) producing a train of pulses of frequency ($1/t_{clk}$) in a period of ($T_{ph}$). This train of pulses is fed to counter and The $Ph^*$ pulse is

used as an enable to that counter to count the number of clock pulses during the period $T_{ph}$. By reading the counter value, phase difference angle can be simply detected as ($\Theta_{act} = 2\pi \frac{Tph}{T}$), where $T_{ph}$ is equal to reading of counter multiplied by ($t_{clk}$), while $T$ is the periodic time of the inverter output voltage.

The phase difference $\Theta_{act}$ is compared with required reference angel $\Theta_{ref}$, which is often zero to assure resonance condition. The phase difference error ($e_1$) is applied to PI controller, and the controller output is used as an input to voltage controlled oscillator (VCO) which generates the suitable switching frequency for the inverter.

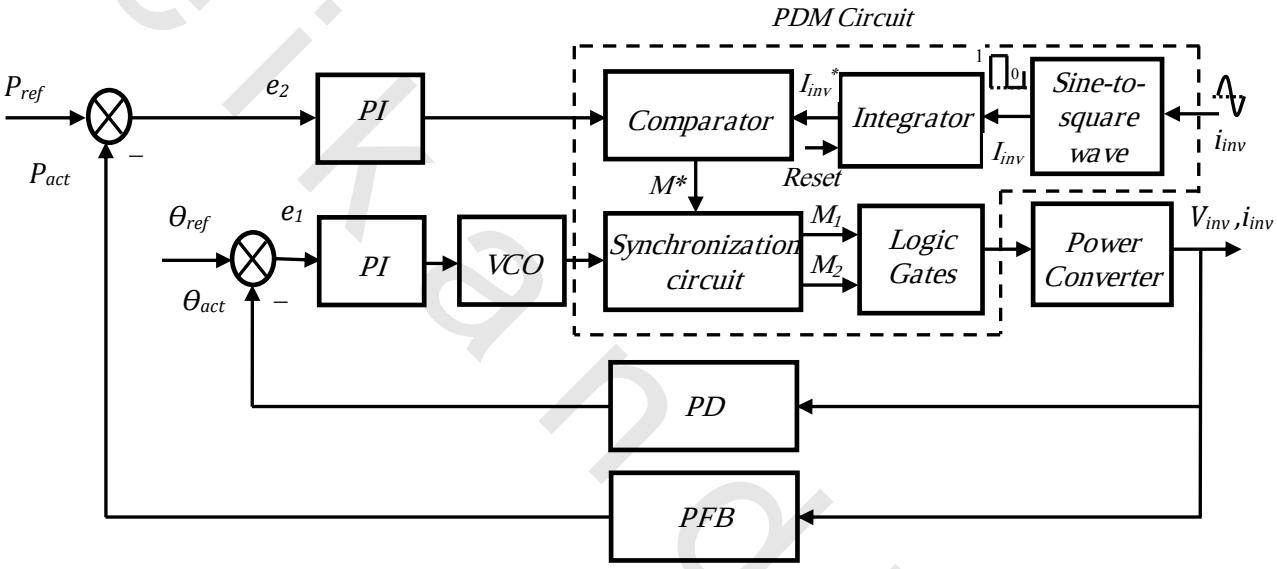



Figure 4.2 Control circuit block diagram for PDM.

The power feedback circuit (PFB), shown in Figure 4.4, is used to compare the reference power $P_{ref}$ with the actual average output power $P_{act}$. The power error ($e_2$) is applied to another PI controller (PFB PI-controller). The PI controller output is compared with saw-tooth signal generated from PDM control circuit (figure 4.5) to generate a square pulse ($M^*$) whose width will completely depend on the PI controller output. Finally, the sinusoidal output of the VCO is converted to unipolar square wave and fed with the output of power feedback PI-controller to the PDM control circuit shown in Figure 4.5. This circuit is responsible for generating the inverter gate pulses as illustrated below.

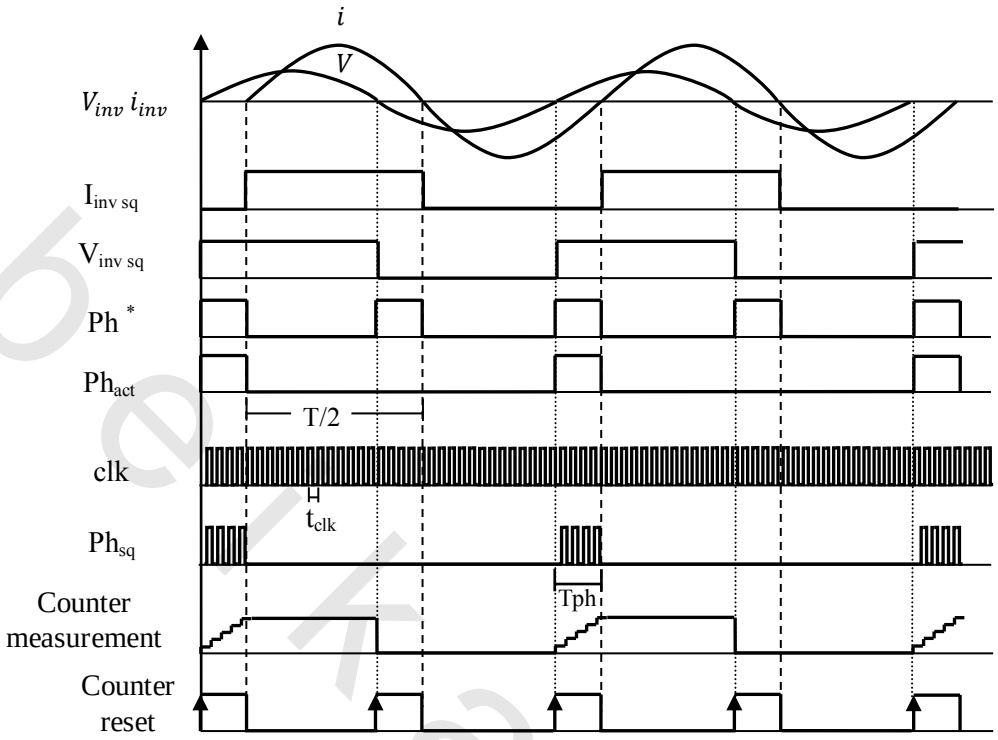



Figure 4.3 Concept of phase detection (PD)

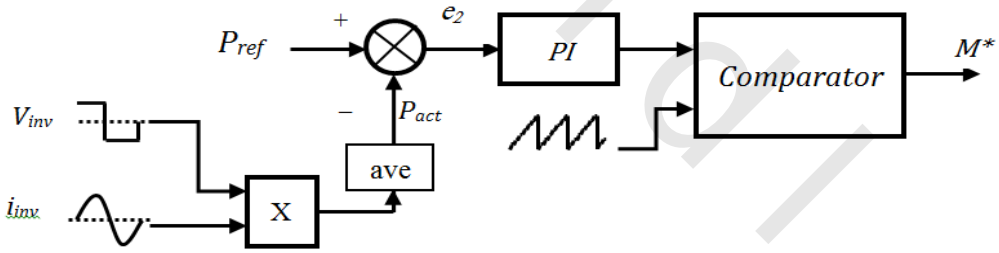



Figure 4.4 Power feedback block diagram

### 4.2.1 PDM control circuit

This circuit generates the inverter firing sequence according to PDM concept. Based on Figure 4.5, the main components of the proposed PDM circuit are:

(i) Integrator,

(ii) Comparator $C_1$,

(iii) Comparator $C_2$,

(iv) Synchronization circuit, and

(v) Simple logic gates.

Figures 4.2, 4.5 and 4.6 illustrate how the PDM pattern can be generated using the proposed approach. The sinusoidal inverter output current ($i_{inv}$) is converted to unipolar square wave ($I_{inv}$), and then it is fed to the integrator. The integrator generates a saw tooth signal ($I_{inv}$*). The integrator output is reset when its output $I_{inv}$* reached to certain predetermined value (which represents the number of desired cycles per $T_{PDM}$). Comparator $C_1$ is responsible for resetting the integrator output. On the other hand, Comparator $C_2$ is responsible for generating the unsynchronized pulses $M$* which is produced by comparing the output of the PFB PI-controller with $I_{inv}$* signal.

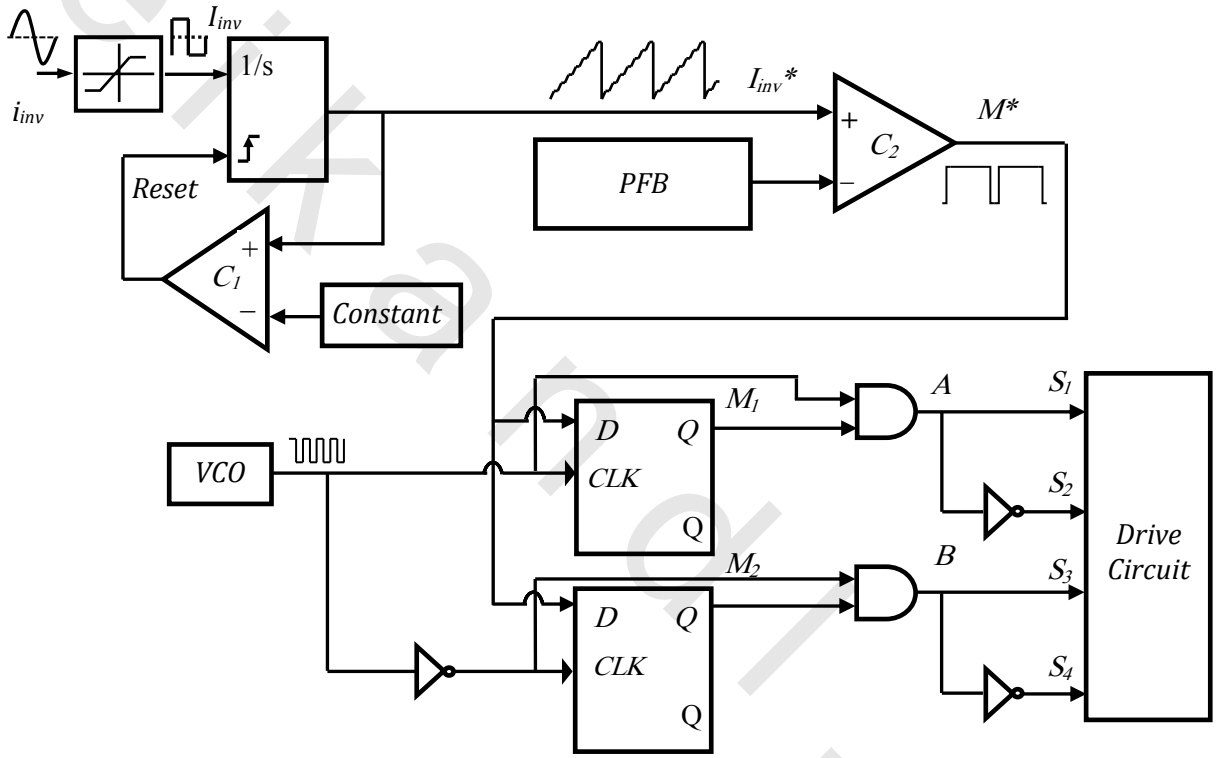



Figure 4.5 PDM pattern generation block diagram

Based on Figure 4.5, the proposed synchronizing circuit (which contains D-type flip-flops) is employed to avoid the change of the current state during the resonant cycle. The VCO output and the unsynchronized pulses $M$* are applied to this synchronizing circuit as clock and data signals, respectively, to hold $M$* until reaching the next rising edge of the VCO output producing a synchronized pulses $M_1$ and $M_2$. These synchronized pulses are fed to simple logic (AND gates) to generate proper gate pulses for the inverter IGBTs (Figure 4.6). The logic gates generate modes I and II alternatively when $M$* = 1, and modes III or IV are developed when $M$*= 0 (zero voltage state mode).

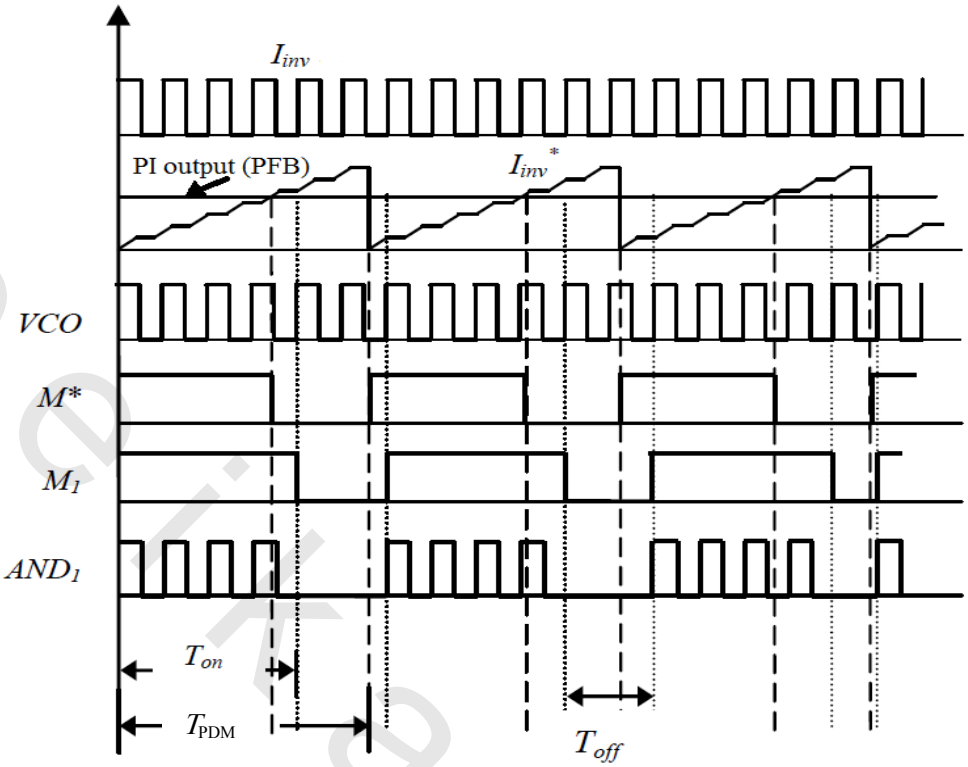



Figure 4.6 Pattern generation signals**.**

## 4.3. SIMULATION AND RESULTS

A simulation model for the proposed PDM controller has been simulated using Matlab/Simulink software package. The detailed power circuit topology is shown in Figure 4.1. An input single-phase AC voltage source of 135 $V_{peak}$ is connected to single-phase uncontrolled rectifier to produce 100 V DC output voltage. The resonant converter with snubber circuits have been implemented using the simpowerSystems Toolbox. A commutating inductor $L_c$ and a commutating capacitor $C_c$ are connected in series with the load equivalent resistance $R_L$ at the output terminals of the single-phase IGBT inverter to form a series resonance inverter.

### 4.3.1 Simulation Model

The proposed controller model is divided into three sub-systems,

(i) Phase difference (PD) sub-system, which detects the phase difference between inverter voltage and current, then compares it with zero as shown in Figure 4.7. The phase difference error is fed to the PI controller to generate the suitable input for the VCO.

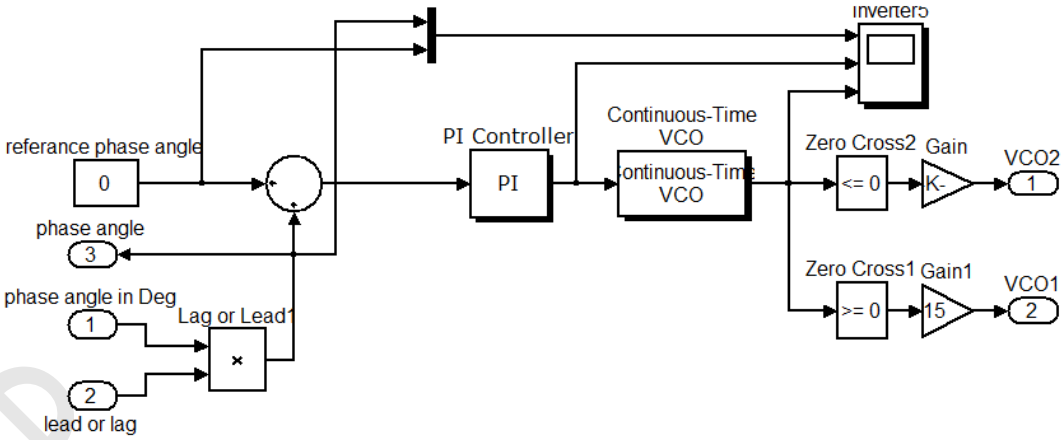



Figure 4.7 Phase angle feedback sub-system

(ii) Power feedback sub-system (PFB) at which the actual output power is calculated and subtracted from the desired output power. The power difference is fed to the other PI controller. The output of power feedback PI controller is used to determine the duration of $T_{on}$ period by comparing its level by the saw-tooth signal ($I_{inv}^{*}$). Figure 4.8 shows the Simulink blocks for power feedback sub-system,

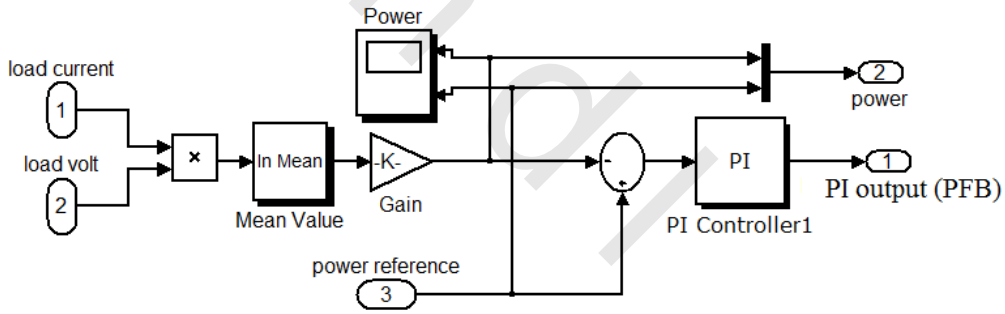



Figure 4.8 Power feedback sub-system

(iii) PDM sub-system: its blocks receive the output of the power feedback PI controller, VCO signals and the inverter output current $i_{inv}$ as shown in Figure 4.2. Figure 4.9 shows the modelling of PDM control sub-system based on the proposed concept.

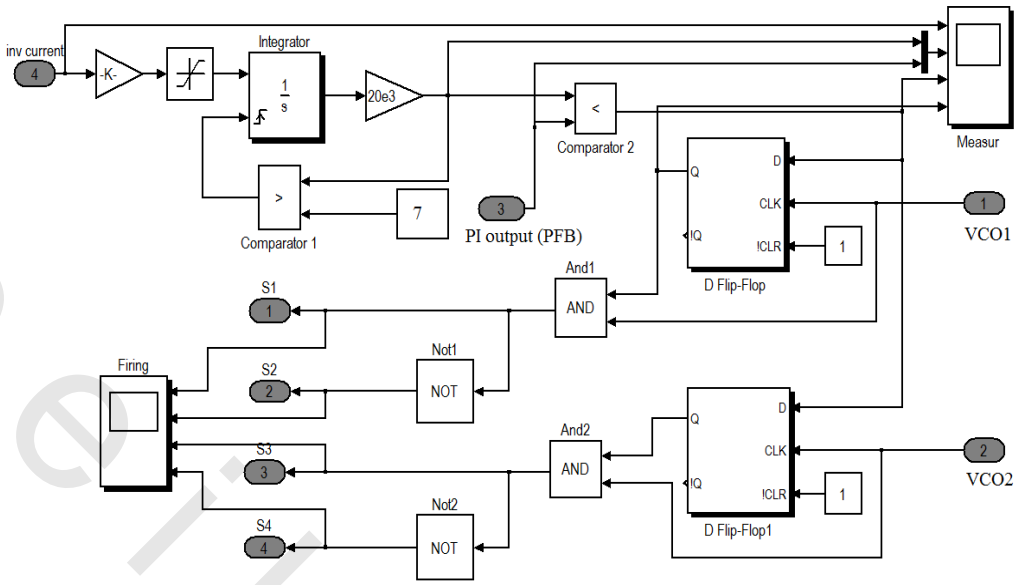



Figure 4.9 PDM control sub-system

### 4.3.2 Simulation Results

In this section, a detailed discussion for the results of the series resonant inverter will be presented when the new proposed controller is enabled. Table 4.1 shows the parameters of the simulated system.

Table 4.1 System Parameters

| Parameter | Description | Value | Unit |
|---|---|---|---|
| $P$ | Desired maximum rated power | 15 | kW |
| $V_{ac}$ | Single phase AC input, peak | 135 | Volt |
| $f_s$ | Switching frequency | 30 | kHz |
| $L_f$ | Filter inductor | 2 | mH |
| $C_f$ | Filter capacitor | 2500 | µF |
| $L_c$ | Series Commutating inductor | 795 | µH |
| $C_c$ | Series Commutating capacitor | 35.3 | nF |
| $C_s$ | Snubber capacitor | 2.2 | nF |
| $R_s$ | Snubber resistance | 100 | Ω |
| $R_L$ | Load equivalent resistance | 0.5 | Ω |

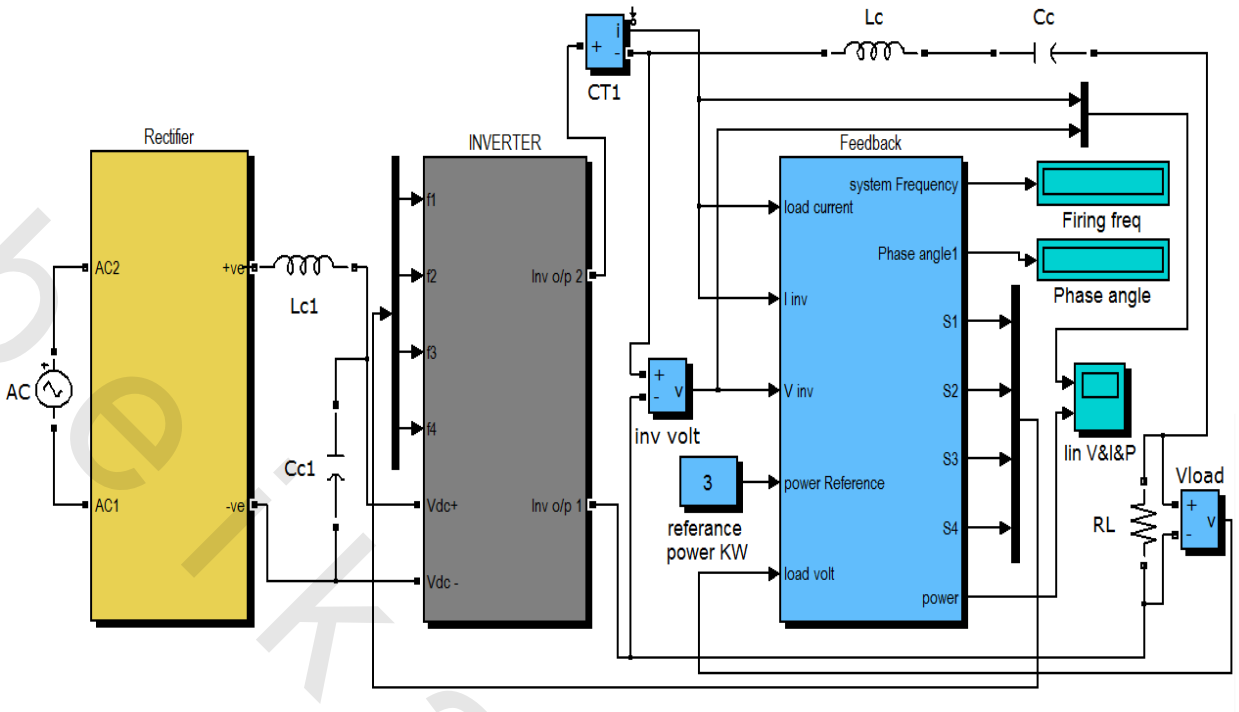
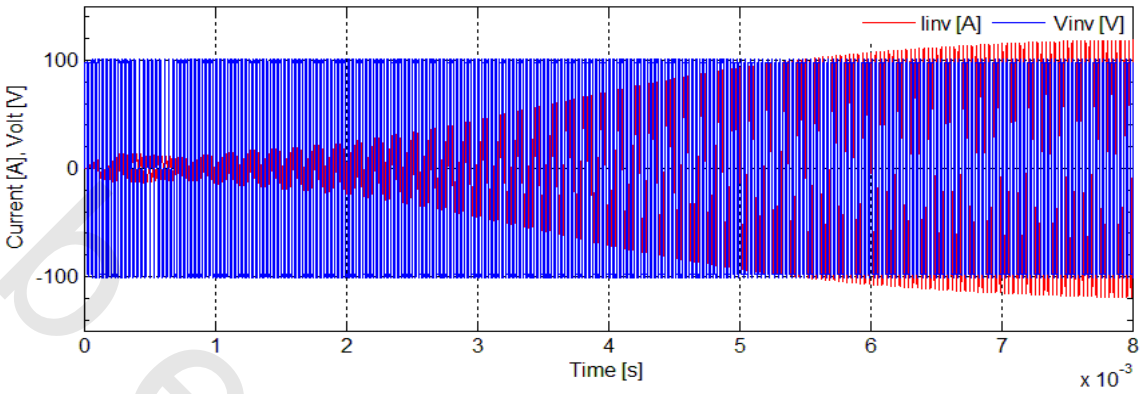


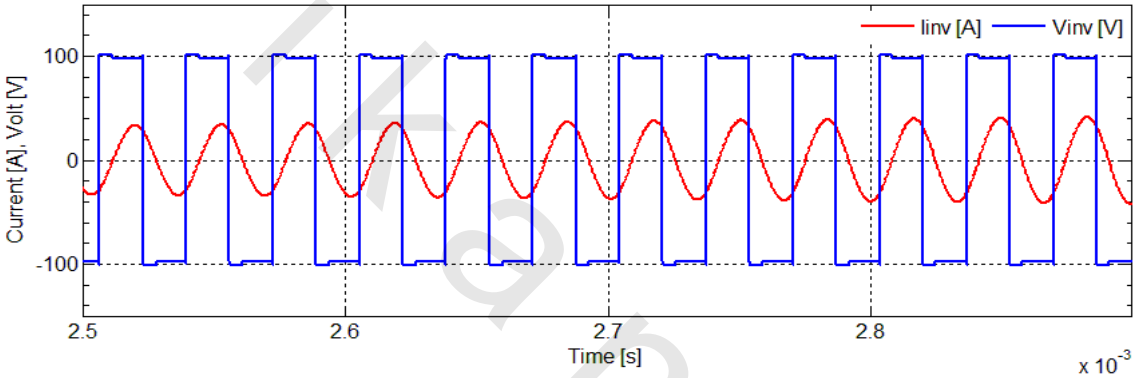

Figure 4.10 The closed loop control of PDM-based induction heating system

Figure 4.10 shows the Simulink model for the closed loop control of PDM-based induction heating system, where the firing pulses of the series resonant converter is controlled using the proposed PDM controller.

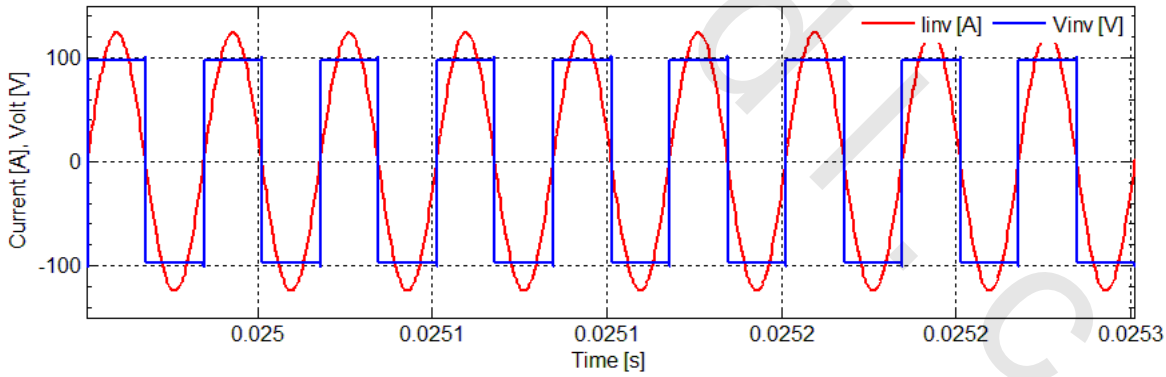
Figure 4.11(a) shows the response of inverter voltage and current at rated power (15 kW). A zoom in view for Figure 4.11(a) ,during starting period, is shown in Figure 4.11(b) where the system power factor is relatively low, while the control system trying to decrease the phase difference between inverter voltage and current. On the other hand, the zoom in view for Figure 4.11(a), during steady state, is shown in Figure 4.11(c). The latter figure shows the system achieves unity power factor (zero phase between $V_{inv}$ and $i_{inv}$), i.e. the switching occurs at the zero current (ZCS). In this case, the pulse density equals one, i.e. there are no off (or stop) cycles.




(a)




(b)

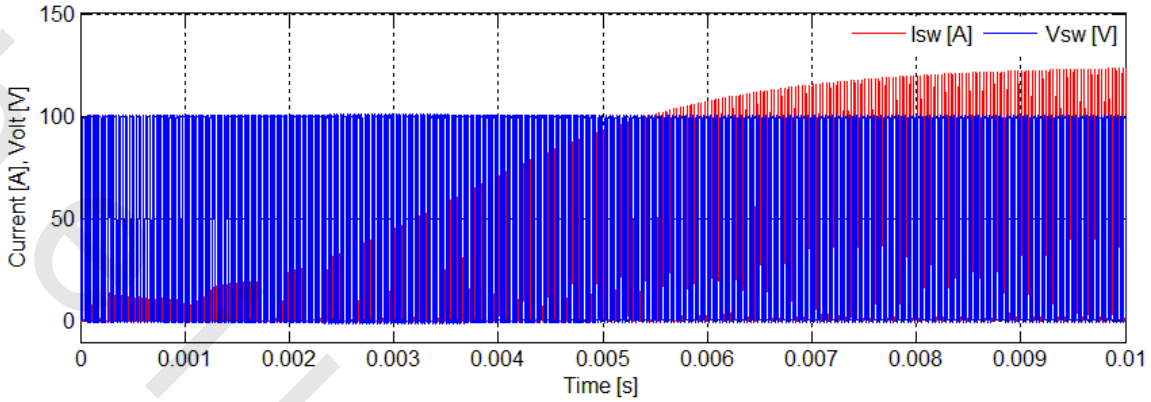



(c)

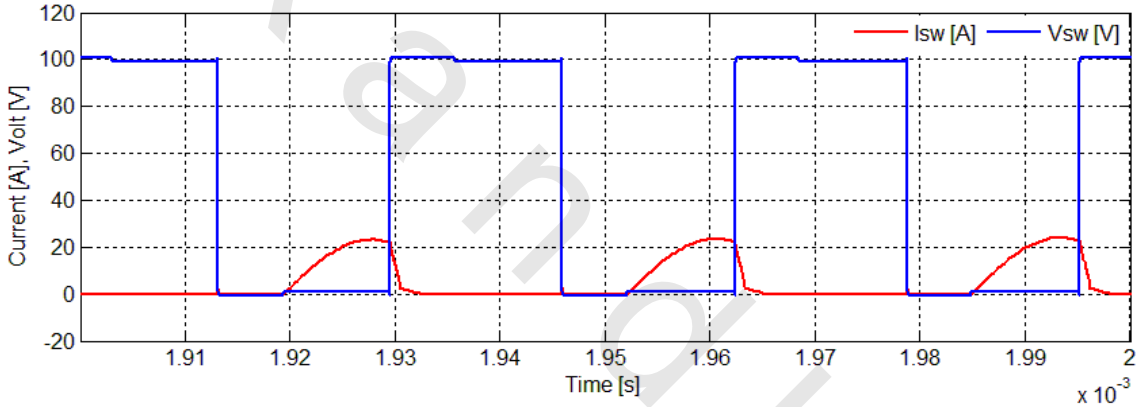
Figure 4.11 (a) Inverter voltage in [V] and current in [A] for output power of 15kW
(b) Zoom in for figure 4.11(a) at starting
(c) Zoom in for figure 4.11(a) at steady state

Figure 4.12(a) shows the response of IGBT voltage and current at rated power (15 kW). A zoom in view for this figure ,during starting period, is shown in Figure 4.12(b) where the phase angle between the switch voltage and current is not zero which exceeds the switching losses. After reaching the steady state condition Figure 4.12(c), the proposed controller decreases the

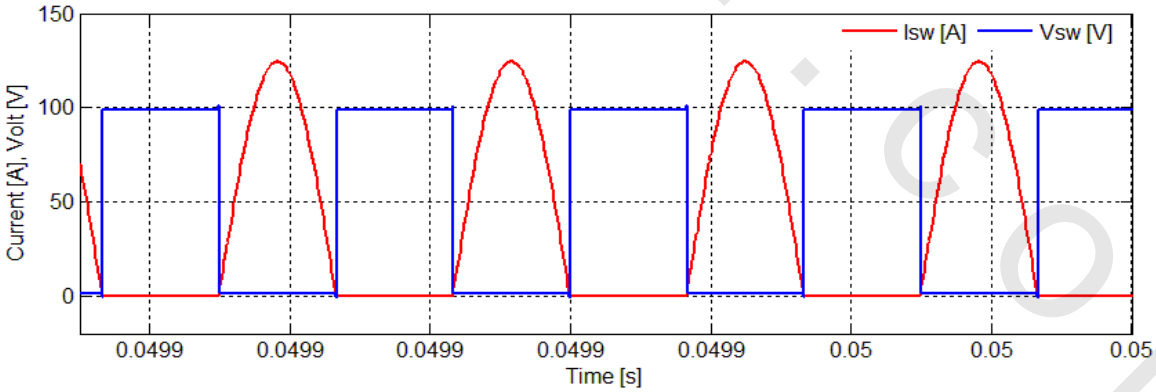
phase angle between inverter voltage and current to zero which reduces the switching losses. Figure 4.13 shows the corresponding supply voltage and current.




(a)




(b)




(c)

Figure 4.12 (a) IGBT voltage in [V] and current in [A] for output power of 15kW
(b) Zoom in for figure 4.12(a) at starting
(c) Zoom in for figure 4.12(a) at steady state

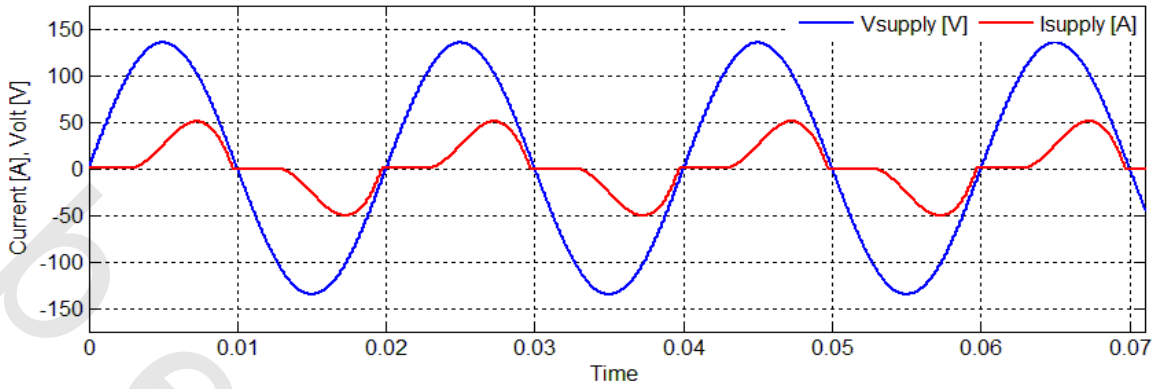



Figure 4.13 Supply voltage in [V] and current in [A] for output power of 15 kW

Figure 4.14 shows the IGBT voltage and current at reference power of 10 kW at steady state, where the phase angle between inverter voltage and current reduced to zero.

Figures 4.15(a), (b), and (c) show the inverter voltage and current at reference power of 10kW, 1kW and 0.2kW respectively, to show the effect of PDM technique on the system response. It is clear for all cases that the inverter voltage is always in phase with current, where the off cycles are 1, 4, and 5 cycles, respectively.

The corresponding output power responses are shown in Figure 4.16. It has to be noted that, the PDM control parameters were adjusted to allow the output power follows the reference power with minimum settling time, minimum overshoot and minimum steady state error.

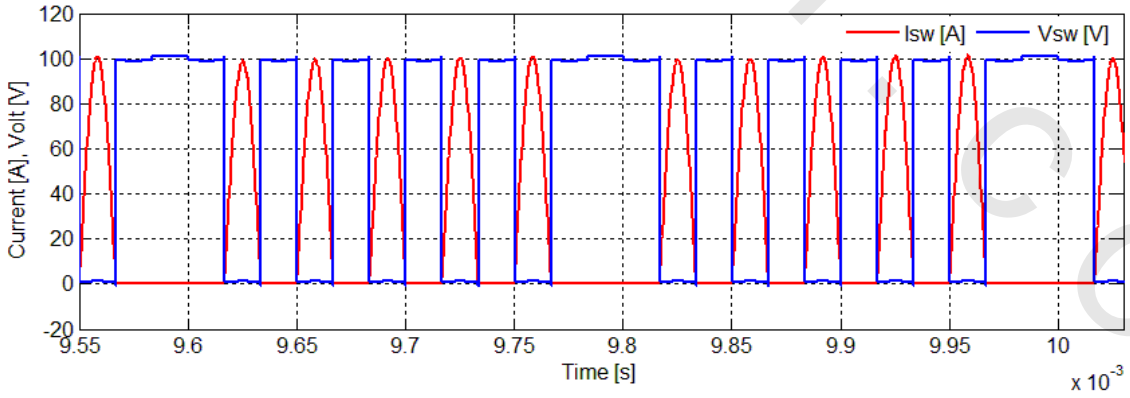
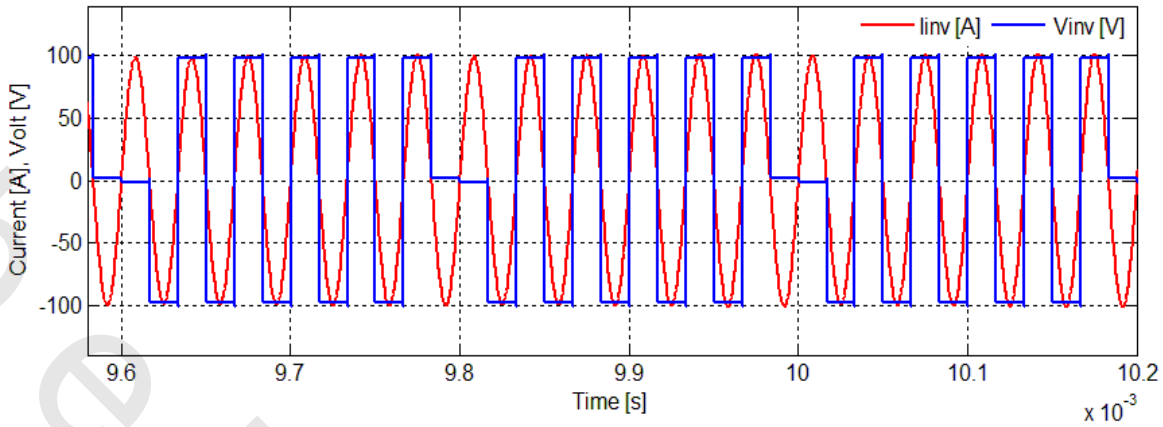
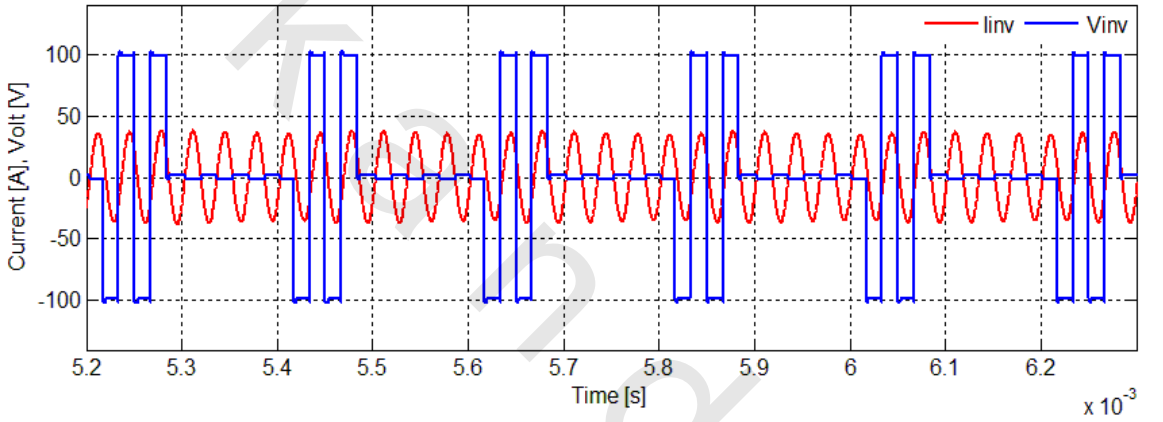


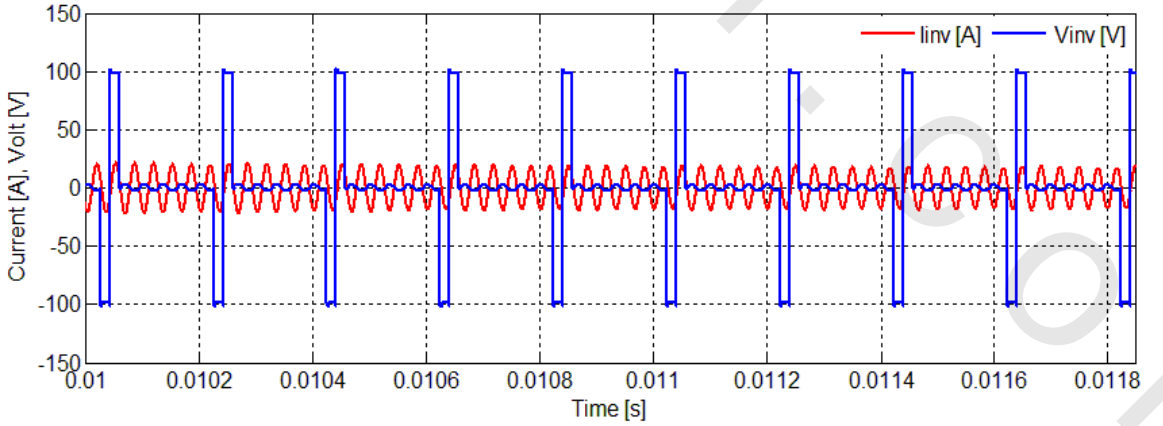

Figure 4.14 IGBT voltage in [V] and current in [A] for output power of 10kW at steady state




(a)

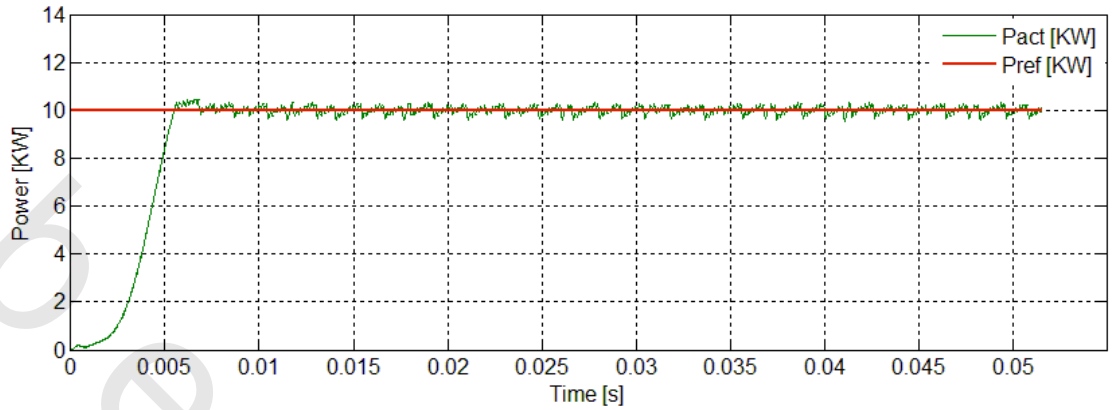



(b)

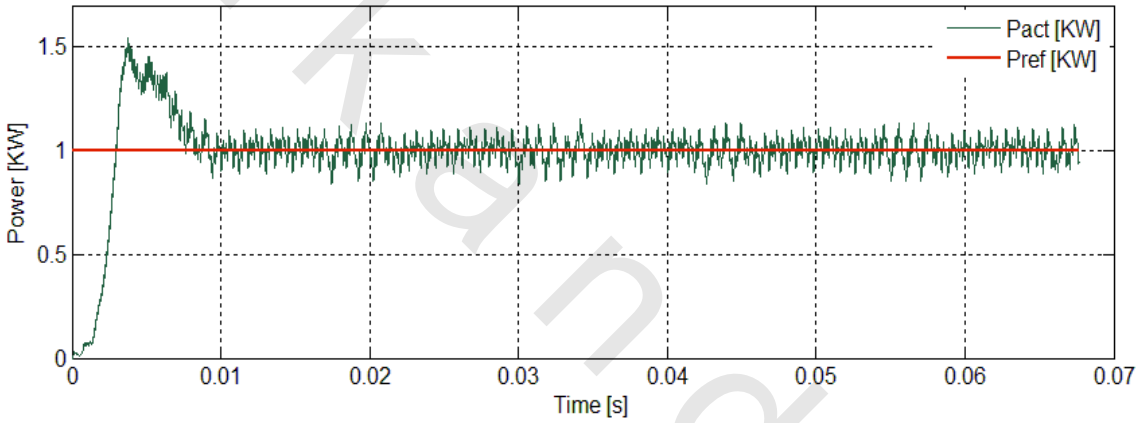



(c)

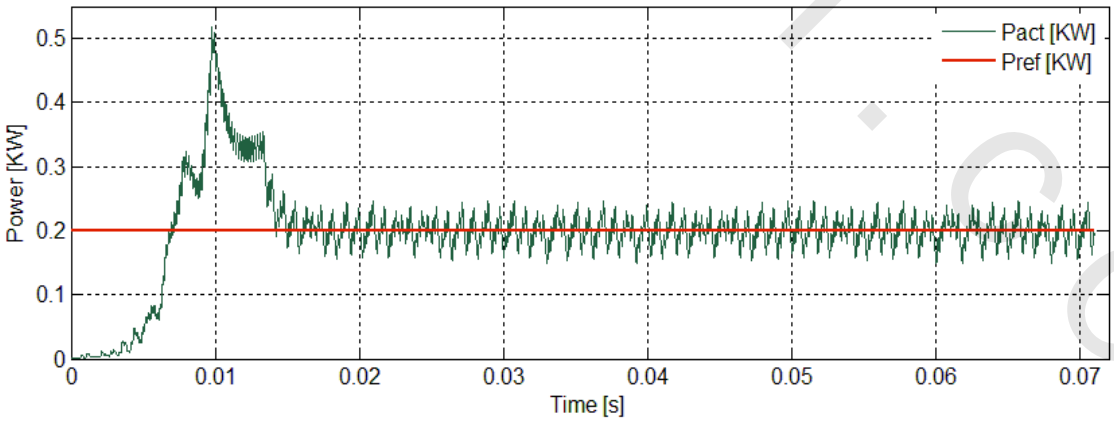
Figure 4.15 Inverter voltage in [V] and current in [A] for output power of (a) 10kW, (b) 1kW, (c) 0.2kW




(a)




(b)




(c)

Figure 4.16 The actual power compared with the reference power for output power of (a) 10kW, (b) 1kW, (c) 0.2kW

Refereeing to section 4.2.1 and Figure 4.6, the PDM pattern generation at output power of 10kW is shown in Figure 4.17, as the modulation index $M$ = 5/6 , i.e. there is only one off cycles.

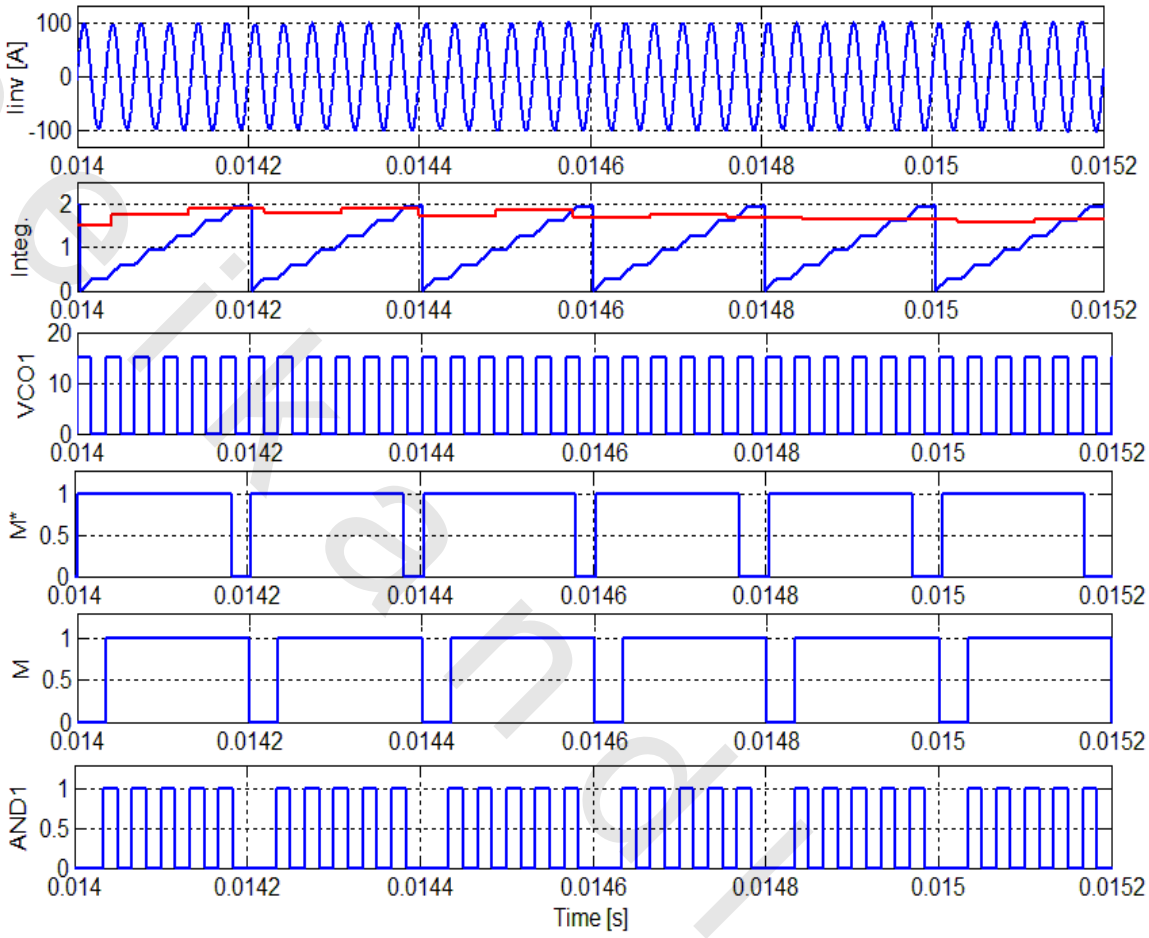



Figure 4.17 PDM pattern generation at reference power of 10 kW

Figure 4.18(a) shows the step response of the heating system for different ranges of reference power (3, 8, 13, 6, 2, 15.5, 10, 0.1 and 0.7 KW). It can be observed that the output power oscillates successfully around the desired value. The corresponding inverter current response is shown in Figure 4.19.

When the reference power changes, the controller tries to adjust the modulation index $M$ to assure tracking of the reference power. This operation has no influence on the phase shift control between the inverter voltage and the current. The corresponding voltage and current waveforms are shown in Figure 4.20, where the effect of the proposed controller is shown by

changing the pulse density of inverter voltage producing a zero voltage cycles, and the inverter current decayed hardly due to the effect of high quality factor (*Q*) of the system.

Based on the presented results, the performance of the new PDM controller is satisfactory, and it is able to track the power reference level successfully with unity power factor (i.e. with minimum switching losses due to ZCS).

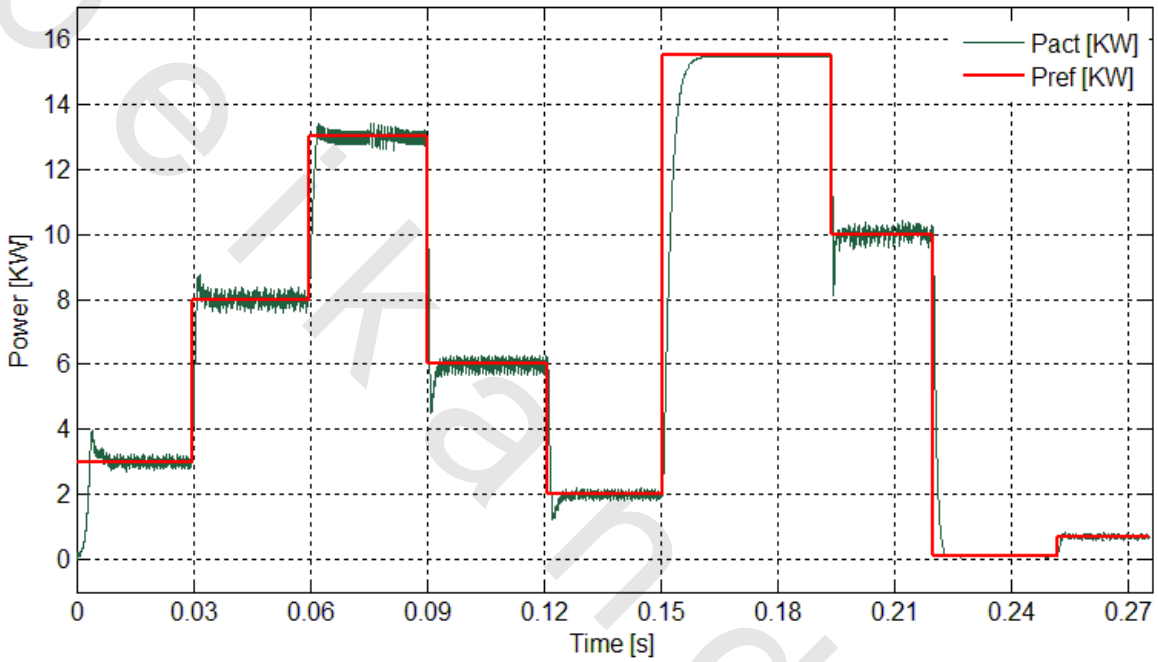



Figure 4.18 step response of the heating system, assuming different power levels

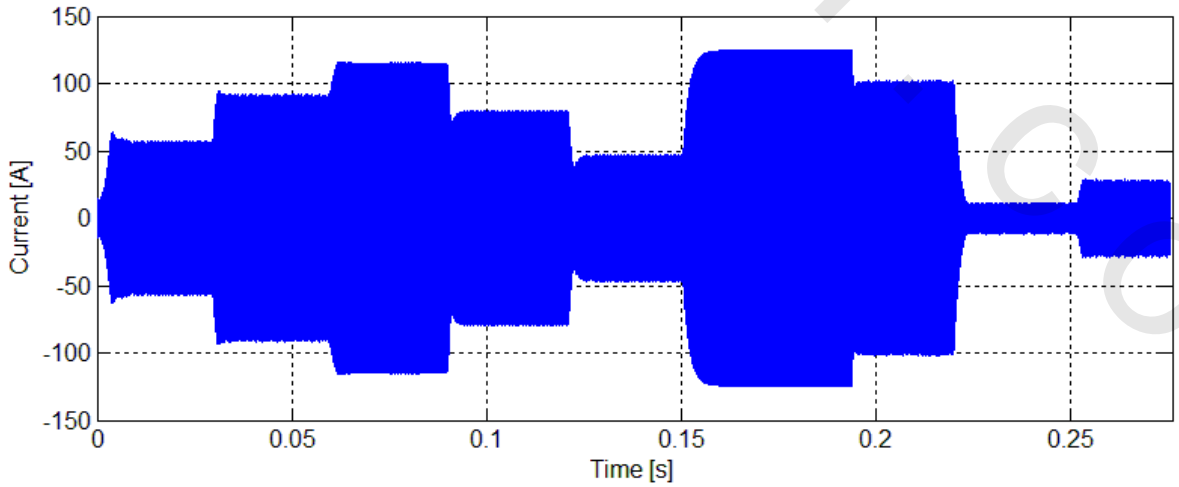



Figure 4.19 Inverter current response for step change in the reference power