CHAPTER 11
PLL Applications

11.1 Quadrature Phase Detector (QPD):

The input is multiplied by the in-phase and the quadriphase VCO outputs through two arms I and Q. The output of the I arm is used as a PD to lock the VCO. When the loop is out of lock, the filtered output of both arms will be the beat frequency, $\sin(\Delta\omega t + \theta)$ for the I arm, and $\cos(\Delta\omega t + \theta)$ for the Q arm, and no dc component is produced.

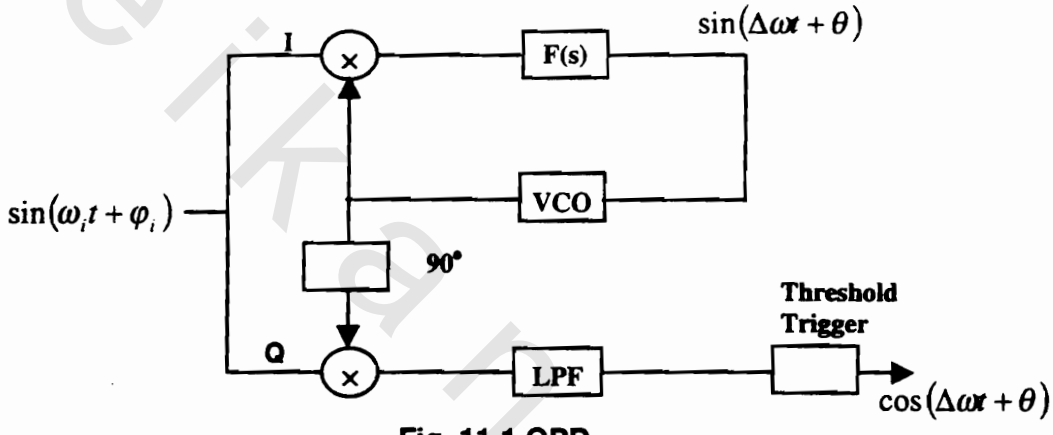


Fig. 11.1 QPD

Under lock condition, $\Delta\omega = 0$, and the output of the I arm is proportional to $\sin\theta$ (or θ, if θ is small). The output of the Q arm is proportional to $\cos\theta$ or (1 if θ is small). Thus, the output of the Q arm will be nearly zero when out of lock, and will have a steady dc voltage when in lock. The LPF in the Q arm has a very small bandwidth. This circuit is often used as a lock indicator. We have noted before that the PLL cannot really discriminate between the case when the loop is locked on ω_0 $(\Delta\omega = 0)$, and the case when the loop is out of lock. In both cases, the output in zero. With QPD, we have a way for such discrimination. In Fig. 11.1, a threshold trigger is added to change the circuit into a true lock-in indicator, which is immune from false alarm. Quite often, this circuit may also be used as an AM detector (Fig.11.2).

The input is $[1 + m(t)]\cos\omega_c t$. We tune the PLL, i.e., $\omega_0 = \omega_c$. Considering the PD to be a multiplier, the output of the VCO is $\cos(\omega_c t + \phi)$. The output of the PD is

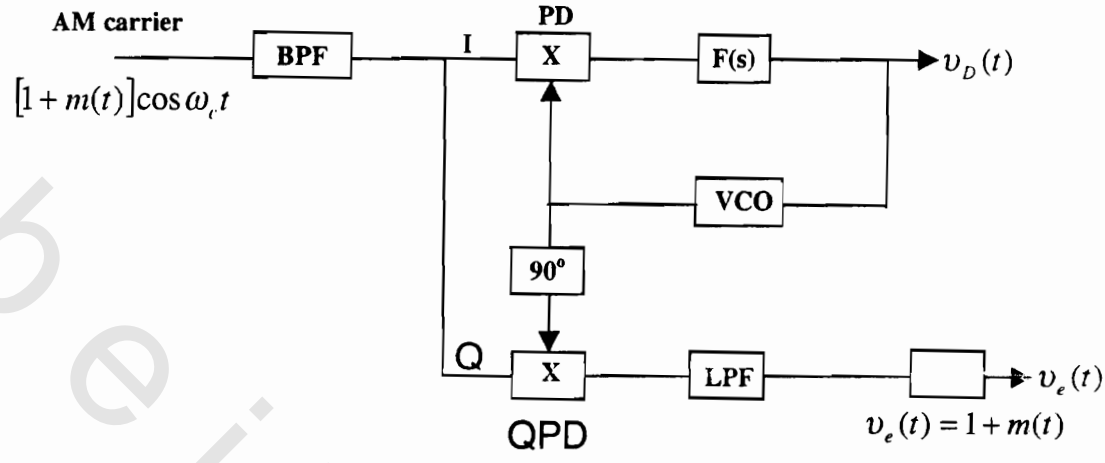


Fig. 11.2 PLL as an AM detector

$$v_D(t) = [1+m(t)]\cos\phi = [1+m(t)]\sin\theta \qquad (11-1)$$

Thus, when $\omega_0 = \omega_c$

$$v_D(t) = 0, \quad \text{for } \theta = 0 \qquad (11-2)$$

The PD output of the I branch is not affected by the AM modulation. However, the output of the Q branch is

$$v_e(t) = k_D[1+m(t)]\cos\theta \qquad (11-3)$$

For $\theta = 0$, at locking

$$v_e(t) = k_D[1+m(t)] \qquad (11-4)$$

Thus, we obtain the modulating signal $m(t)$, superimposed on a dc voltage of the lock indicator.

This type of amplitude demodulation is coherent, since it is realized by multiplying the input with a recovered carrier from the VCO in phase with the transmitted carrier. This is called carrier tracking.

11.2 Signal Synchronizers: Costas Loop

As we know, the carrier is often suppressed to make a more efficient transmission scheme. Accurate reception requires the regeneration of the carrier in frequency and phase synchronism. These circuits are called signal synchronizers. PLLs are often used in such circuits. PLL applications discussed earlier require an input signal at the frequency to be tracked. Signal synchronizers employ a nonlinear circuit to regenerate a carrier, or clock signal, together with a PLL to track the signal. An example circuit is shown in Fig. 11.3. The incoming signal is squared and then passed through a narrow BPF tuned to $2\omega_c$

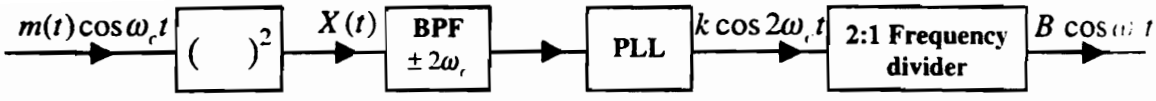


Fig. 11.3 Generation of a coherent carrier using signal squaring

The squarer output $X(t)$ is

$$X(t) = [m(t)\cos\omega_c t]^2 = \frac{1}{2}m^2(t) + \frac{1}{2}m^2(t)\cos 2\omega_c t \qquad (11-5)$$

Now, $m^2(t)$ is a nonnegative signal, and thus, the signal has an average value, while $m(t)$ itself has a zero average value.

Let us assume

$$\frac{1}{2}m^2(t) = k + \psi(t), \qquad (11-6)$$

where k is a dc value, and $\psi(t)$ is a zero mean baseband signal. Thus, from eqn. (11.6), eqn. (11.5) becoms.

$$X(t) = k + \psi(t) + k\cos 2\omega_c t + \psi(t)\cos 2\omega_c t \qquad (11-7)$$

The PLL acts as a narrowband high Q BPF tuned to $2\omega_c$. It suppresses all of the components in eqn. (11.7), and only $k\cos 2\omega_c t$ is picked up. A divider 2:1 gives $B\cos\omega_c t$. This method determines frequency synchronism, but loses phase synchronism.

Another circuit solves this problem. It is called Costas loop (Fig.11.4). Here, the PLL acts as a very high Q BPF, requiring very little bandwidth, and hence, generating minimal noise. The incoming signal is $m(t)\cos(\omega_c t + \phi_i)$. At the receiver, a VCO generates the carrier $\cos(\omega_c t + \phi_o)$. The two LPFs suppress high frequency terms to yield $m(t)\cos\theta$ and $m(t)\sin\theta$. These outputs are further multiplied to give $\frac{1}{2}m^2(t)\sin 2\theta$.

When this is passed through a narrow BPF, the output is $K\sin 2\theta$, where K is the dc component of $\frac{1}{2}m^2(t)$. The signal $K\sin 2\theta$ is applied to the input of a VCO. Thus, the loop has delivered the demodulated signal $m(t)$ (when $\theta = 0$) through the generation of a coherent carrier. Note that θ measures the variation from the null point $\Delta\phi = \pi/2$.

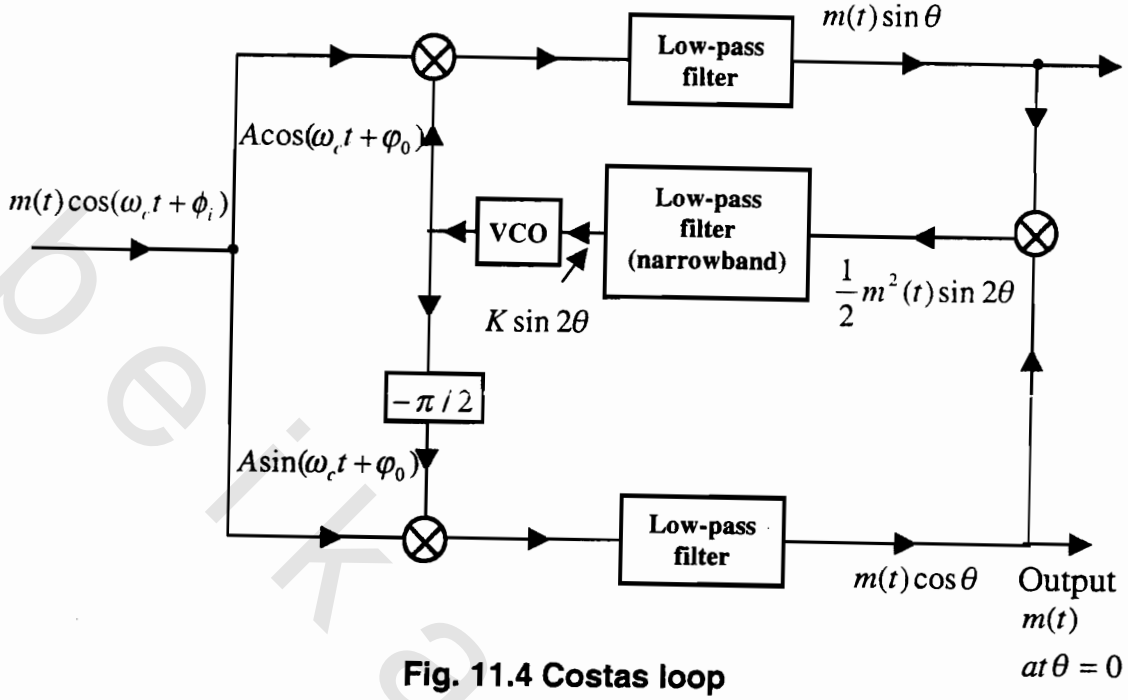


Fig. 11.4 Costas loop

Ex. 11.1:

Design a touch tone decoder. The combination of tones are prescribed by the following table.

Low group Hz	Digits		
697	1	2	3
770	4	5	6
852	7	8	9
941	*	0	#
High group (Hz)	1209	1336	1477

Seven PLL's are required, and the center frequency of each VCO is adjusted for one of the seven transmitted tones. Note that the separation between the frequencies in each group is about 10%, so that the loop bandwidth should not exceed 5%. The choice of the loop BW is a compromise between the desired safeguard against false lock to an adjacent frequency and the drift of the VCO center frequency with time and temperature. The correct combination of PLLs to produce the required digit is shown in Fig. 11.5.

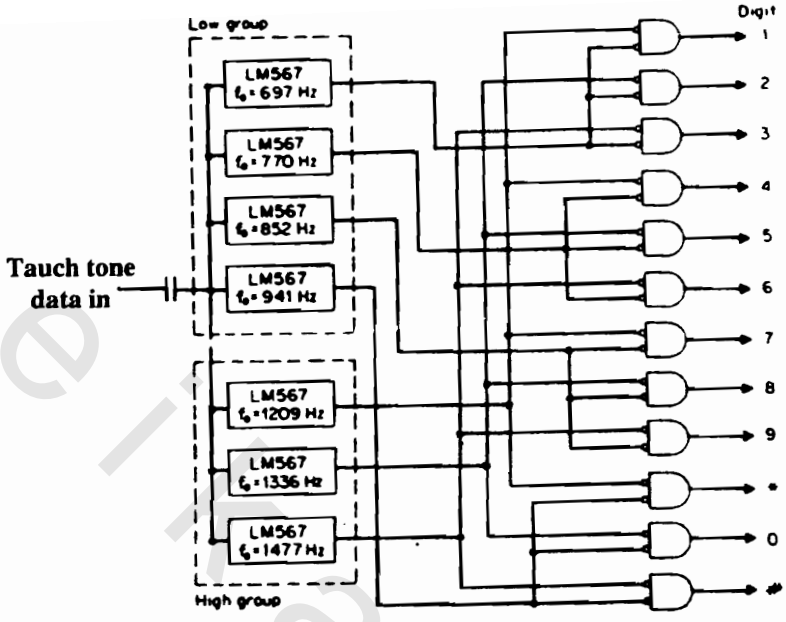


Fig. 11.5 PLL tone decoders

11.3 Frequency Synthesizers:

A frequency synthesizer is a frequency source whose output is an integer multiple of an input reference frequency. It is formed from a PLL by breaking the connection between the VCO and the phase detector with a divide by N counter. The counter generates a single output pulse for every N input pulses. The phase detector output voltage after filtering controls the output frequency of the VCO (Fig. 11.6). When the loop is locked, the output frequency $f_o = Nf_r$, where f_r is the reference frequency, and N is a programmable counter setting. While this simple approach is often adequate for low frequency applications, it has a severe drawback, namely the programmable counter has to divide the VCO output directly.

Due to delays in the feedback path, counters usually have an upper limit. It is recommended, therefore, to use a fixed prescaler (divider) and divide both the reference and VCO frequencies by M (Fig.11.7), so that f_O / M is within the counting range of the programmable counter. The disadvantage of this approach is that the large division ratio with feedback loop reduces the PLL loop gain by increasing the response time to a change in the counter setting.

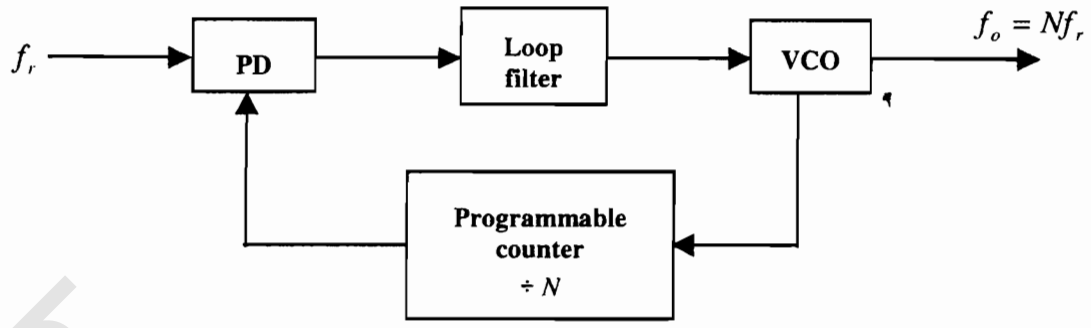


Fig. 11.6 Direct frequency synthesizer using a PLL

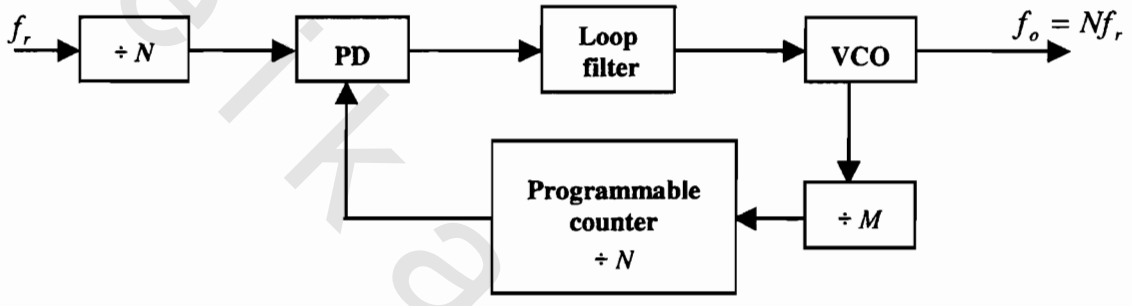


Fig. 11. 7 Frequency synthesis with prescaling of reference and output frequencies.

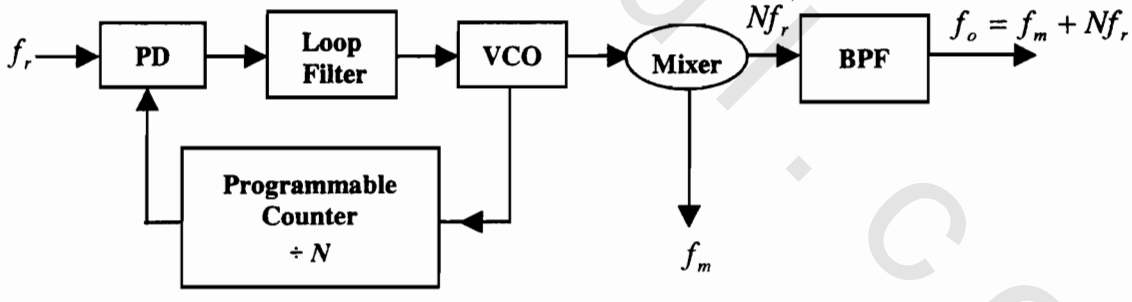


Fig. 11.8 Frequency synthesizer using a PLL and a mixer

As a solution to this problem, the VCO frequency is mixed with a stable offset frequency f_m, to obtain the desired output frequency $f_0 = f_m + Nf_r$ (Fig. 11.8).

The input reference frequency f_r is usually less than 10kHz. The actual frequency reference - which is a stable crystal oscillator - usually operates from 1-10 MHz. The divide by N counter - placed between the crystal oscillator and the PD - may be set at 100, for crystal oscillator frequency f_x of 1 MHz, to produce 10 kHz input reference.

A second technique known as heterodyne down conversion (Fig.11.9) uses a second crystal oscillator (called an offset or local oscillator f_H) feeds to a mixer stage, where it is mixed with the output frequency f_O. The resultant output is the difference f_{mix}:

$$f_{mix} = f_o - f_H \qquad (11-8)$$

This difference is fed to the $\div N_2$ counter, where maximum and minimum values are given by

$$N_{2\max} = \frac{f_{mix,\max}}{f_r} = \frac{f_{o\max} - f_H}{f_r} \qquad (11-9)$$

$$N_{2\min} = \frac{f_{mix,\min}}{f_r} = \frac{f_{o\min} - f_H}{f_r} \qquad (11-10)$$

$$f_o = f_H + N_2 f_r \qquad (11-11)$$

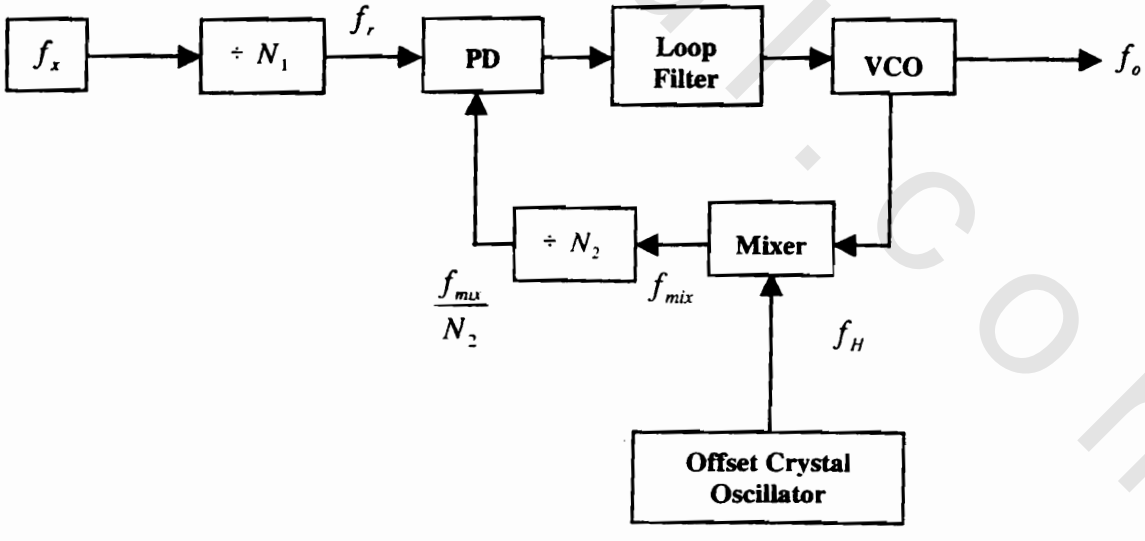


Fig.11.9 Heterodyne down conversion

Ex. 11.2:

Two hundred FM broadcast channels are to be equally spaced 100 kHz apart in the range of 88-108 MHz. The FM receiver uses 10.7 MHz IF .Design the local oscillator used in the FM receiver. Repeat this problem using prescaling with a 1MHz crystal controlled reference and a 98 MHz offset .

Solution:

This synthesizer is the local oscillator used in the FM receiver to tune 88-108 MHz input frequencies to produce 10.7 MHz IF. The output frequency of the synthesizer must tune from 88 + 10.7 = 98.7 MHz to 108 + 10.7 = 118.7 MHz. For a channel spacing of 100 kHz, f_r (the 1MHz reference) must be reduced by a factor of 10. This means N_1 = 10. From eqns. (11.9) and (11.10),

$$N_{2\max} = \frac{f_{o_{\max}} - f_H}{f_r} = \frac{118.7 - 98}{0.1} = 207$$

$$N_{2\min} = \frac{f_{o_{\min}} - f_H}{f_r} = \frac{98.7 - 98}{0.1} = 7$$

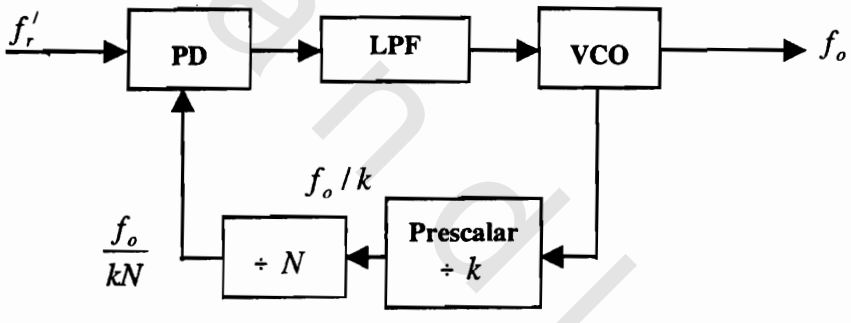


Fig. 11.10 Frequency synthesizer using a prescalar

Thus, the output of the local oscillator f_O is given by eqn. (11-11):

$f_o = f_H + N_2 f_r$, where N_2 varies from 7 to 207.

$$f_r' = \frac{f_o}{kN} \qquad (11-12)$$

$$f_o = Nkf_r' \qquad (11-13)$$

We call

$$f_{ch} = kf_r' \qquad (11-14)$$

$$f_o = Nf_{ch} \qquad (11-15)$$

$$N = \frac{f_o}{f_{ch}} \qquad (11-16)$$

$$N_{\max} = \frac{f_{o_{\max}}}{f_{ch}} \qquad (11-17)$$

$$N_{\min} = \frac{f_{o_{\min}}}{f_{ch}} \qquad (11-18)$$

Here, in this problem.

$$f_{ch} = 100kHz$$

Take

$$f_r' = 10kHz,$$

Thus,

$$k = \frac{f_{ch}}{f_r'} = \frac{100}{10} = 10$$

$$N_{\max} = \frac{f_{o_{\max}}}{f_{ch}} = \frac{118.7}{0.1} = 1187$$

$$N_{\min} = \frac{f_{o_{\min}}}{f_{ch}} = \frac{98.7}{0.1} = 997$$

Ex. 11.3:

Four hundred FM channels are to be equally spaced 10 kHz apart, so that the reciever tunes from 144 to 148 MHz. The output of the synthesizer is multiplied by 9 and added to 10.7 MHz. The input reference frequency is derived from a 4.551111 MHz oscillator and divided by 12. The synthesizer must have programmed inputs ranging from 400 ($N_{2\min}$) at 144 MHz to 800 ($N_{2\max}$) at 148 MHz. Determine the frequency of the local oscillator. Then, resolve this problem using prescaling.

Solution:

The reference frequency $f_r = \frac{4.551111}{2^{12}} MHz = 1.11111\ kHz$

For the receiver to tune from 144 to 148 MHz, the output frequency of the synthesizer f_O must lie between $f_{o_{\min}}$ and $f_{o_{\max}}$

$$f_{o_{\min}} = \frac{144 - 10.7}{9} = 14.811111MHz$$

$$f_{o_{\max}} = \frac{148 - 10.7}{9} = 15.255555MHz$$

$$f_H = f_{o_{\max}} - N_{\max} f_r = 15.255555 - 800\text{X}1.11111 = 14.366667MHz$$

11.4 Steady State Linearized Analysis of Frequency Synthesizer:

When the loop is locked, from Fig. 11.11,

$$f_r = f_d = \frac{f_0}{N} \tag{11 - 19}$$

or

$$f_0 = Nf_r \tag{11 - 20}$$

Since the phase is the time integral of frequency,

$$\theta_d = \frac{\theta_0}{N} \tag{11 - 21}$$

From the feedback loop, we have

$$\frac{f_r'(s)}{f_0(s)} = \frac{\theta_0(s)}{\theta_r(s)} = \frac{k_d\ k_0\ F(s)/s}{1 + k_d\ k_0\ F(s)/Ns} \tag{11 - 22}$$

If no LPF is used,

$$\frac{\theta_0(s)}{\theta_r(s)} = \frac{k_d\ k_0}{s + k_d\ k_0/N} = \frac{N\ k_v'}{s + k_v'} \tag{11 - 23}$$

where

$$k_v' = \frac{k_d\ k_0}{N} \tag{11 - 24}$$

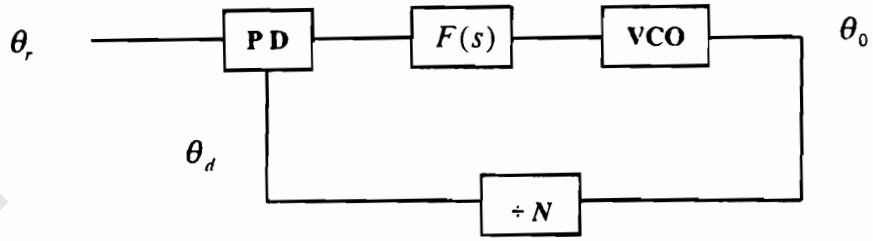
This is the angular bandwidth of the frequency synthesizer of the first order loop. For typical values of k_d of 2V/rad, k_O 100 rad/Vs and $N = 40$ (as an example of designing 1 MHZ from 25 kHz reference), we find the bandwidth to be 5 Hz. The loop behaves as a narrow BPF. It is easier to build a narrow bandwidth circuit using a PLL than with high Q filters. When we use a LPF of the form.

$$F(s) = \frac{1}{1 + \frac{s}{\omega_L}} \tag{11 - 25}$$

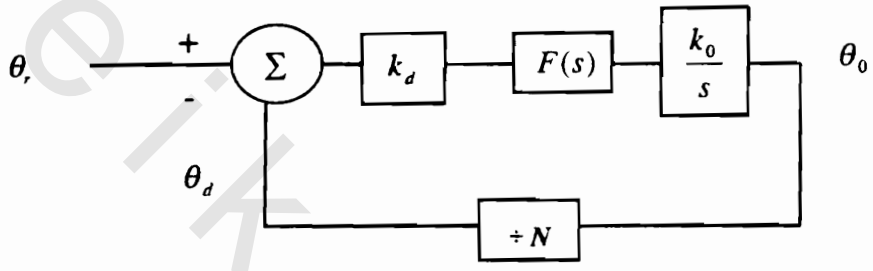
$$\frac{\theta_0(s)}{\theta_r(s)} = \frac{N\ k_v'}{s\left(\frac{s}{\omega_L} + 1\right) + k_v'} = \frac{N}{\frac{s^2}{\omega_n^2} + \frac{2\xi\ s}{\omega_n} + 1} \tag{11 - 26}$$

$$\omega_n^2 = k_v'\ \omega_L \tag{11 - 27}$$

$$2\xi = \frac{\omega_n}{k_v'} = \left(\frac{\omega_L}{k_v'}\right)^{1/2} \tag{11 - 28}$$



(a)



(b)

Fig. 11.11 Frequency synthesizer loop
a) block diagram b) linear model

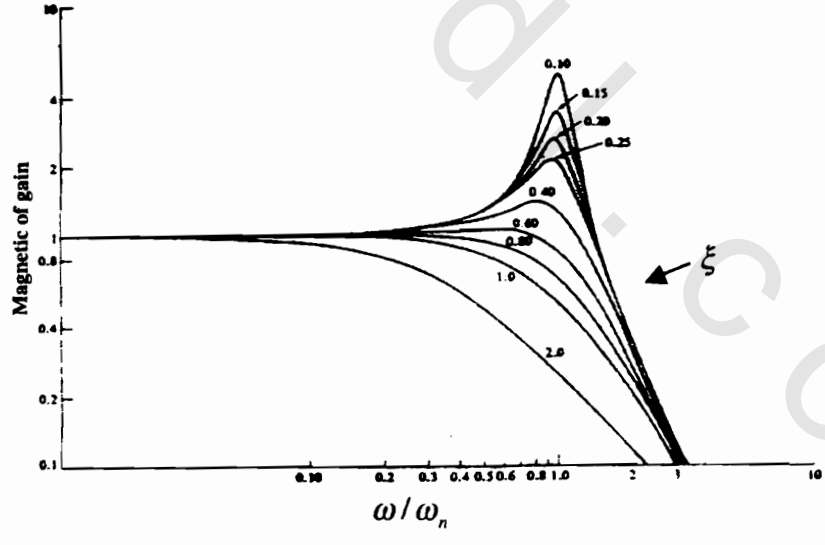


Fig. 11.12 Transfer function of frequency synthesizer loop of second order

$$\left|\frac{\theta_0(j\omega)}{\theta_r(j\omega)}\right| = \frac{N}{\left[\left(1-\frac{\omega^2}{\omega_n^2}\right)^2 + \left(2\xi\frac{\omega}{\omega_n}\right)^2\right]^{1/2}} \qquad (11-29)$$

$$\arg\frac{\theta_0(j\omega)}{\theta_r(j\omega)} = -\tan^{-1}\frac{2\xi\omega}{\omega_n(1-\omega^2/\omega_n^2)} \qquad (11-30)$$

For ξ=0.707, the transfer function becomes the second order maximally flat Butterworth response. For ξ<0.707, the gain exhibits peaking in the frequency domain. The peak response M_p is given by

$$M_p = \frac{N}{2\xi(1-\xi^2)^{1/2}} \qquad (11-31)$$

which occurs at

$$\omega_p = \omega_n(1+2\xi^2)^{1/2} \qquad (11-32)$$

The 3dB frequency ω_h can be derived as

$$\omega_h = \omega_n\left[1-2\xi^2+(2-4\xi^2+4\xi^4)^{1/2}\right]^{1/2} \qquad (11-33)$$

The time taken for the output to rise from 10-90% (called rise time t_r) is

$$t_r = \frac{2.2}{\omega_h} \qquad (11-34)$$

Again, we would like to have the bandwidth as narrow as possible for maximum filtering, and have the rise time as short as possible, so that the loop can follow changes in the input waveform (Prob 11.8). A compomise is usually made.

11.5 Stereo demodulator:

A small amplitude carrier (pilot) is at one half of the carrier frequency (19 kHz) is also transmitted. At the receiver, a PLL operates on the 19 kHz pilot carrier to produce a 38 kHz signal. This 38 kHz carrier will be in synchronism with the original carrier and is combined with the multiplexed stereo signal in the product detector. The output of the product detector then passes through a LPF to produce the L-R signal. The L+R signal is rejected by the LPF. Then, the L-R signal can be combined with the L+R signal to produce the L and R signals for stereo sound.

11.6 PLL Tuner:

The PLL is a key element in modern tuning systems for VHF and UHF electronic tuners (Fig. 11.14)

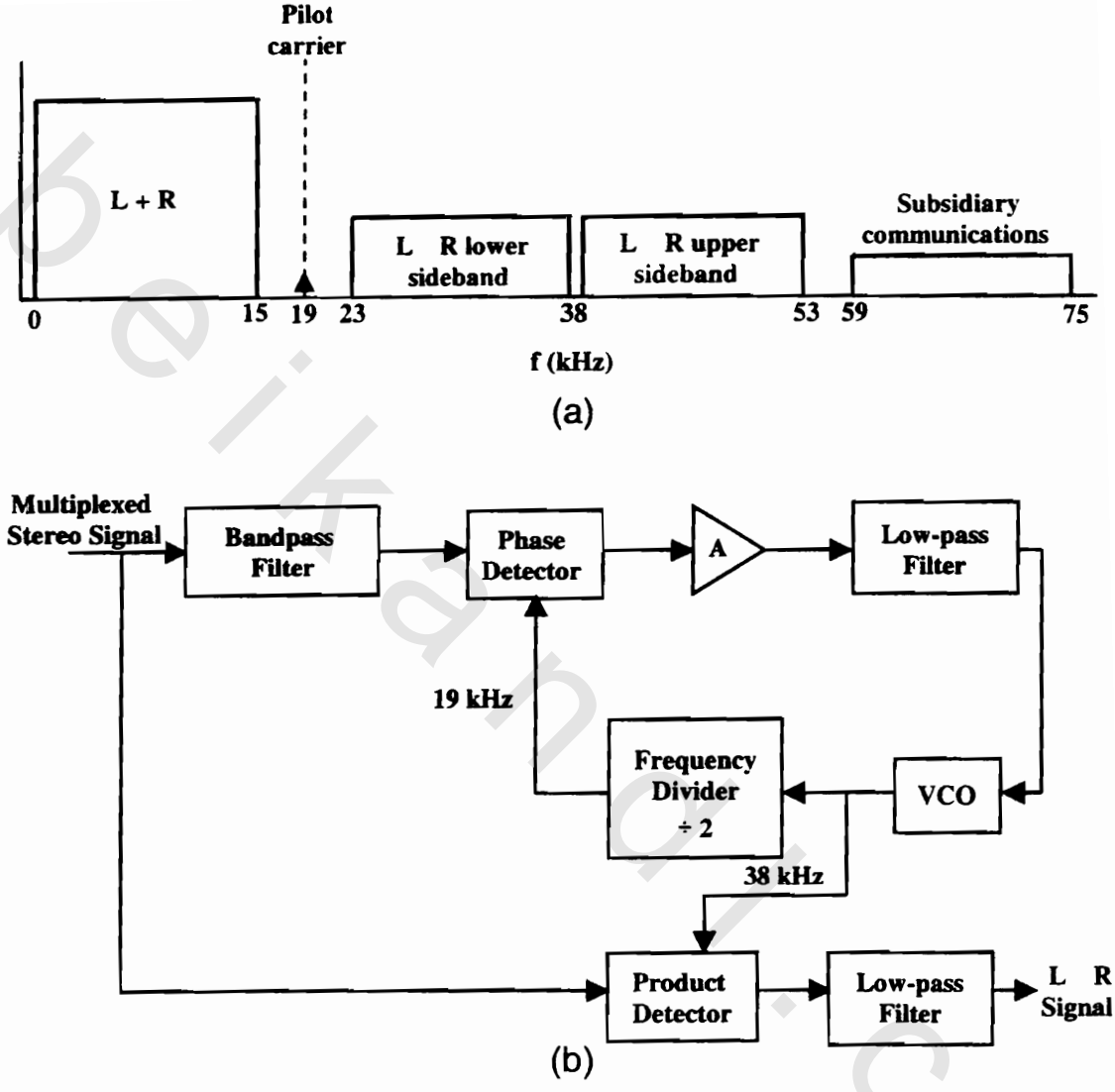


Fig.11.13 Stereo demodulator
a) spectrum b) block diagram

The output of a stable 3.581055 MHz crystal oscillator is applied to dividers to establish a reference frequency input to the phase comparator. The crystal oscillator frequency is divided by a factor of 3667, giving a crystal stable 976.5625 Hz reference frequency to the phase comparator. The local oscillator of the tuner produces a signal that is frequency divided, and compared to the crystal controlled reference frequency. If the frequency of the signal is exactly the same, the phase comparator develops a correction voltage. This voltage is used to adjust the frequency of the tuner oscillator, so that

the two inputs to the phase comparator are exactly at the same frequency. The crystal controlled reference oscillator frequency is always 3.581055 MHz, but the tuner oscillator frequency differs for each channel. If, for example, we have 82 channels, then the system must provide for each of the 82 channels the proper frequency division between the local oscillator in the tuner and the comparator. This is accomplished using a programmable divider.

The local oscillator signal from the VHF or UHF tuner is amplified and applied to a prescaler. The bias voltage B+ is applied to the proper tuner (VHF or UHF). The prescaler is a fixed divide by 256. This means that its output (local oscillator frequency) is divided by 256. Then, it is applied to a fixed divide by 4 divider and a programmable divider. The signal obtained by frequency dividing the local oscillator signal must be exactly the same as the reference frequency. However, the frequency of the local oscillator is different for each channel. Thus, it is the programmable divider that must provide the frequency division for each channel, by supplying the right binary number from a microcomputer.

Since the reference frequency is 976.5625 Hz for the selected channel to be correctly locked in, the tuner oscillator frequency must have a divide by the value of 976.5625 Hz. Thus,

$$\frac{\text{Tuner oscillator frequency}}{256 \times 4 \times N} = 976.5625 \qquad (11-35)$$

The variable N determines the binary inputs to the programmable divider.

Ex. 11.4:

For a PLL tuner, show how channels are switched among channel 2 (101 MHz), channel 6 (129 MHz), channel 3 (275 MHz), and channel 83 (931 MHz).

Solution:

From eqn. (11.35), for channel 2, we have

$$\frac{101\ 000\ 000}{256 \times 4 \times N} = 976.5625\ Hz$$

$$N = \frac{101\ 000\ 000}{1\ 000\ 000} = 101\ ,$$

which is the same as the tuner oscillator frequency in MHz. We thus use $N = 101$. We work backwards

$$\frac{101 \times 10^6}{256 \times 4 \times 101} = 976.5625\ Hz$$

Thus, the value N for any channel is given by

$$N = \frac{\text{Tuner oscillator frequency}}{256 \times 4 \times 976.5625}$$

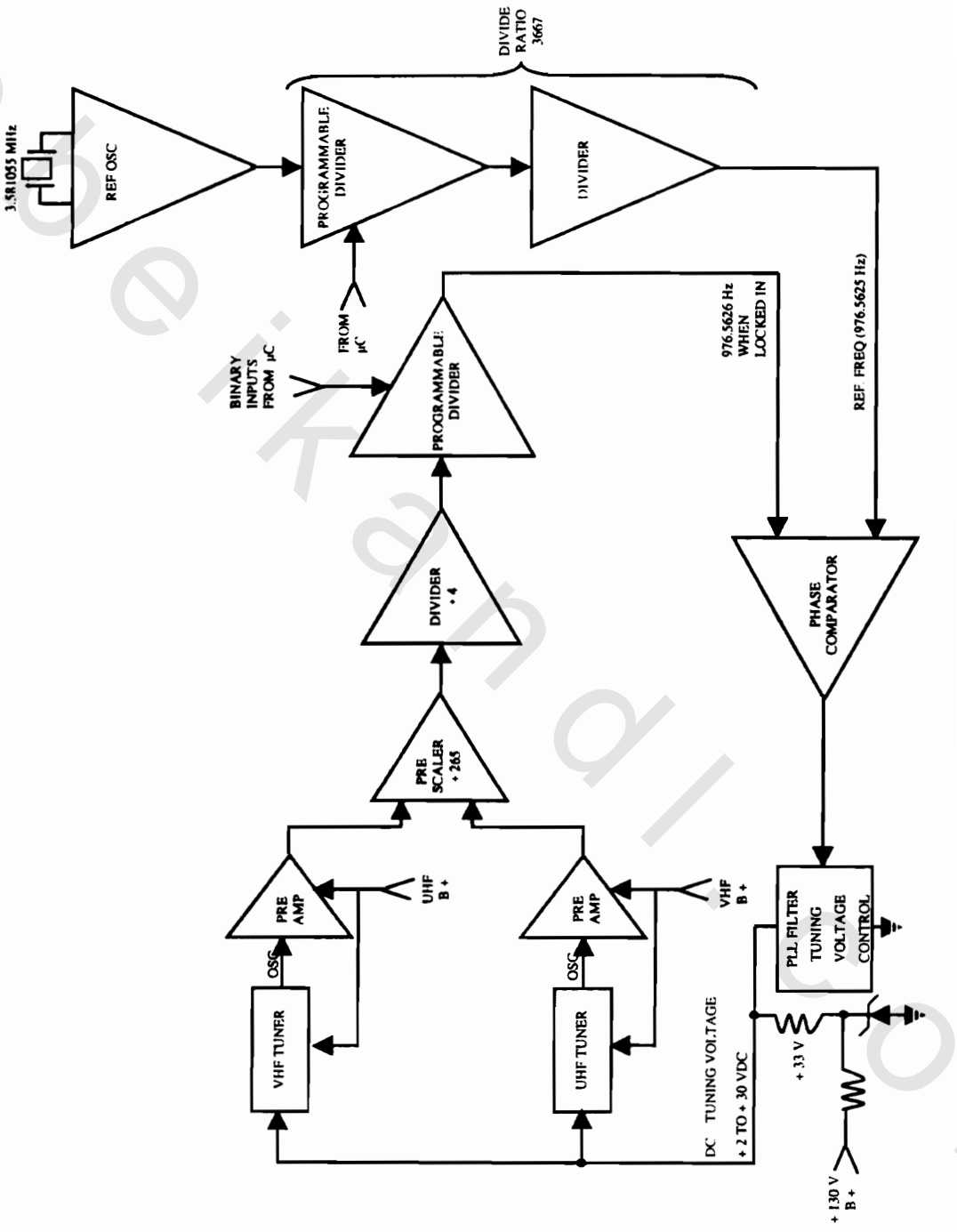


Fig. 11.14 PLL electronic tuning system

For channel 6 (129 MHz), N =129
For channel 13 (257 MHz), N =257
For channel 83 (931 MHz), N =931

As long as both inputs to the phase comparator have equal frequency at 976.5625 MHz, no correction voltage is developed by the comparator. However, if the tuner oscillator frequency drifts, its input to the phase comparator changes. The phase detector develops a dc correction voltage which is fed to the VHF or UHF tuner VCO to correct the frequency.

When the binary input set for a particular channel is changed to switch to another channel, a frequency difference exists between the two comparator inputs. This difference develops a correction voltage which in turn forces the tuner local oscillator to the new frequency, until the two inputs to the comparator will once again be at exactly the same frequency. The way this is done is that any frequency difference between the comparator inputs produces a series of pulses at its output. These pulses must be filtered to produce a dc control voltage, which adjusts the tuning voltage. The diagram of the PLL filter and tuning voltage control circuit is shown (Fig. 11.15)

The +130 V dc input is clamped to +33 V dc by the Zener diode. This establishes the maximum varactor tuning voltage. If there is a frequency difference between the two phase comparator input signals, the phase comparator produces a series of dc pulses at its output at the difference frequency (since we can look at the phase comparator as a multiplier with limiting characteristics or using a digital PD, as in the next section). These pulses are integrated or filtered and applied into the base bias voltage for transistor Q_{58}. Transistors Q_{58} and Q_{59} are connected, so that the conduction of Q_{58} provides a base drive for Q_{59}, where Q_{59} and R_{48} function as a variable resistance between the varactor tuning voltage and ground. Increasing the drive decreases the tuning voltage, and decreasing the base drive increases the tuning voltage. The output voltage to the varactor ranges from +2 to +30 V dc.

A static phase difference exists between the two comparator input signals, where the frequencies are identical and only a slight phase displacement provides a small Q_{58} base current to maintain Q_{58} on (fixing its bias), as required to maintain the desired tuning frequency, and the PLL locked. In other words, we have created a mechanism for locking, while we have the possibility of switching among channels and relocking.

11.7 Digital Phase Detectors

The multiplying PDs are useful for sinusoidal inputs. In the case of digital inputs, digital PDs may be used. The simplest form of a digital PD is the exclusive OR. The output A is high if one of the two inputs is high.

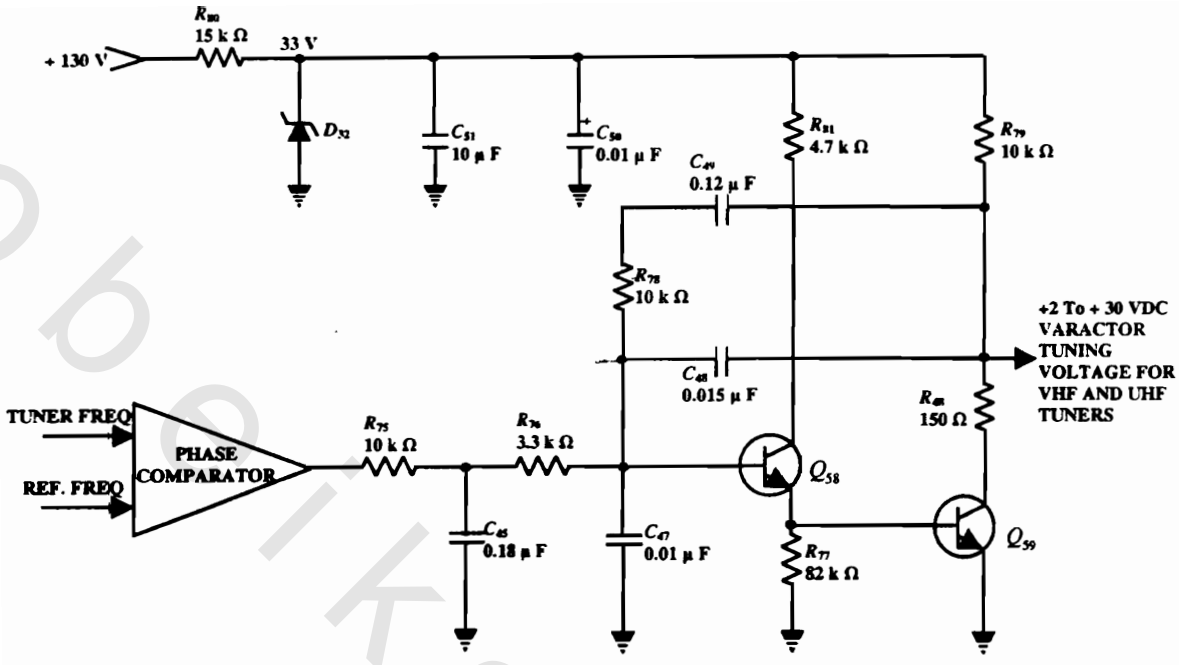


Fig. 11.15 PLL filter and tuning voltage circuit

This PD has triangular characteristic and is linear over the range 0 to π. The steady state phase error is $\pi/2$ for the loop to operate at the center of its linear region. The average output is zero at $\pi/2$. The output frequency is double the input frequency. If one of the inputs is zero all the time, the output average is zero, i.e., at the center of the operating range. The V/2 voltage shifts the operating point for zero phase shift to $\pi/2$ rather than zero. The filter acts as an integrator (Fig. 11.16)

Fig. 11.17 shows an improved version of a digital PD. Here, the positive going edges of the input $V_1(t)$ sets a D flip flop, and the positive going edge of $V_2(t)$ toggles the flip flop, because of the feedback connection of $\overline{Q}$ to D. The input/output relation is a sawtooth, and is linear over the rang o – 2π.

The average output is zero at π. In the absence of input $V_1(t)$, the output is zero. The output frequency is identical to the input frequency.

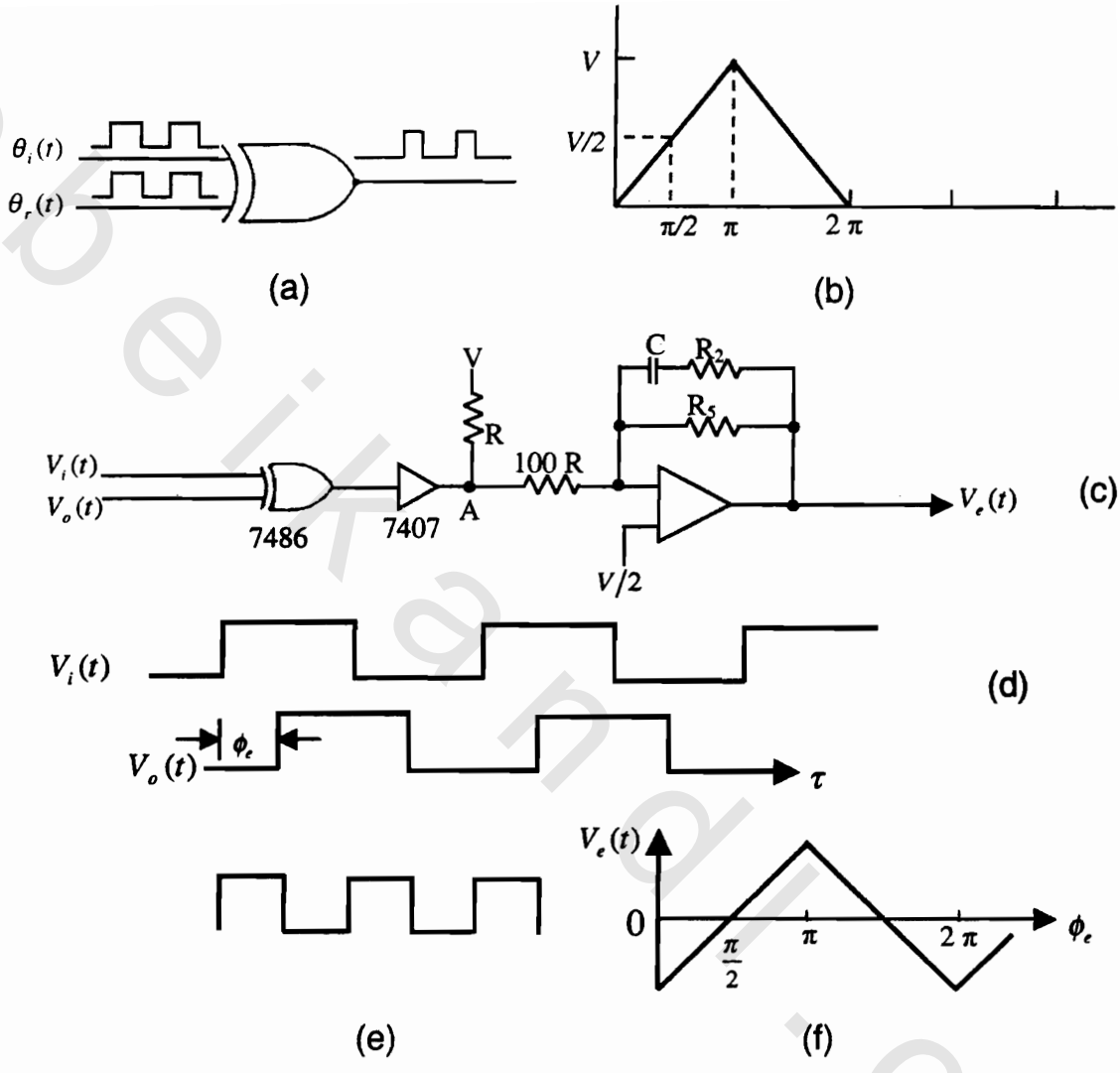


Fig. 11.16 XOR gate as a digital PD

a) simple circuit b) output waveform
c) a practical circuit d) input waveform
e) output at A f) average output as a function of ϕ_e

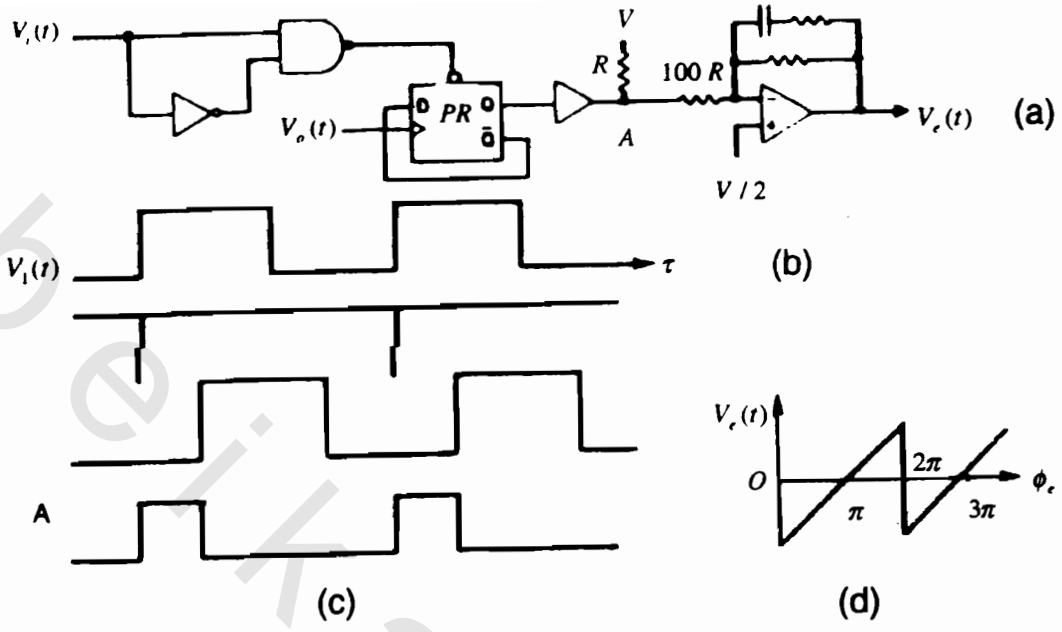


Fig. 11.17 Digital PD with a D flip flop
a) circuit b) waveform
c) output at A d) average output voltage

An alternative is shown in Fig. 11.18. Here, both $V_1(t)$ and $V_2(t)$ clock 1 into two separate D flip flops. However, a NAND gate senses when both flip flops are high, and then resets both of them. The output of the filter is the difference between the outputs of the two flip flops.

This PD has a steady dc output when the frequency f_1 of $V_1(t)$ is different from f_2 of $V_2(t)$. The polarity of this dc output depends on whether f_1 is greater or less than f_2. Thus, the circuit acts as a digital frequency detector. and the frequency detector output is used in aiding acquisition in the PLL. When $f_1 = f_2$, the circuit acts as a phase detector, and its input/output shows a linear relationship over the range -2π to $+2\pi$. The steady state phase error is zero for operations at the center of the operating region.

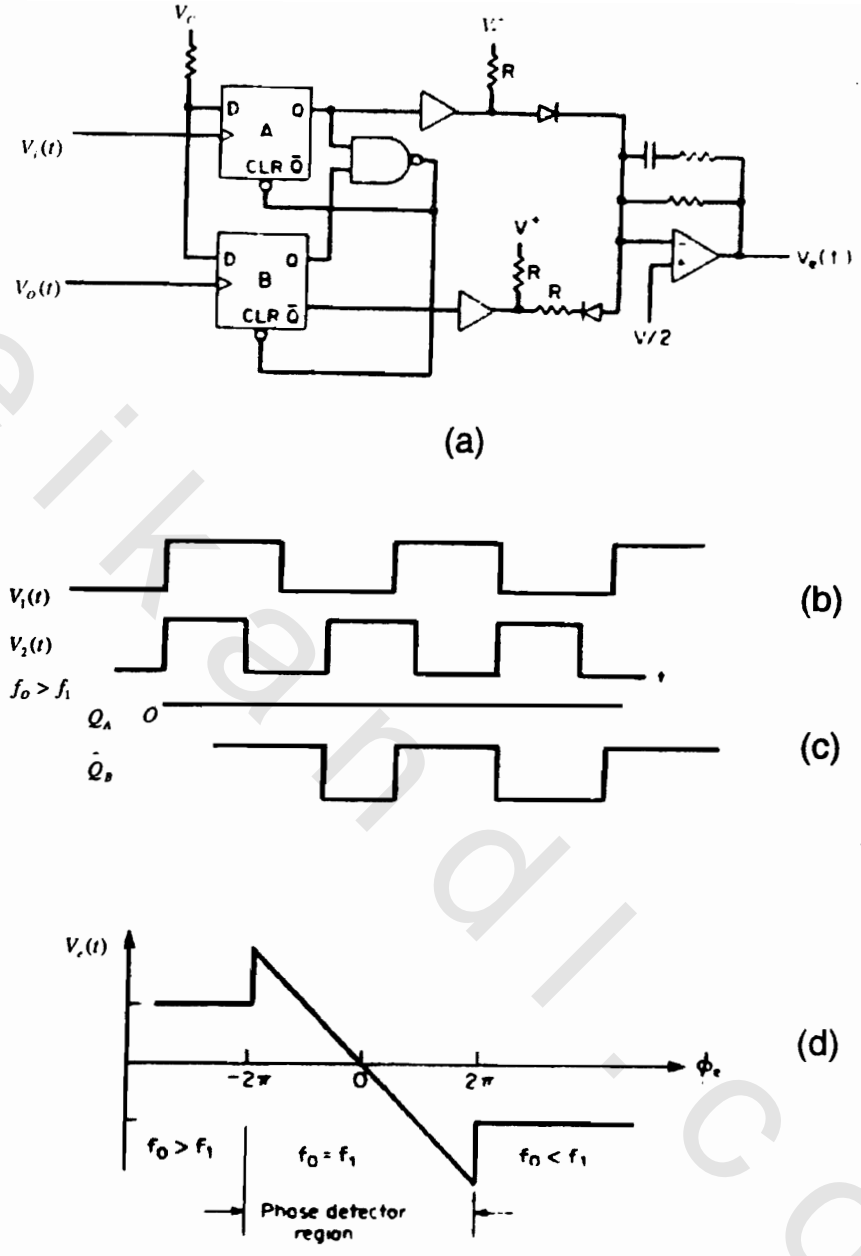


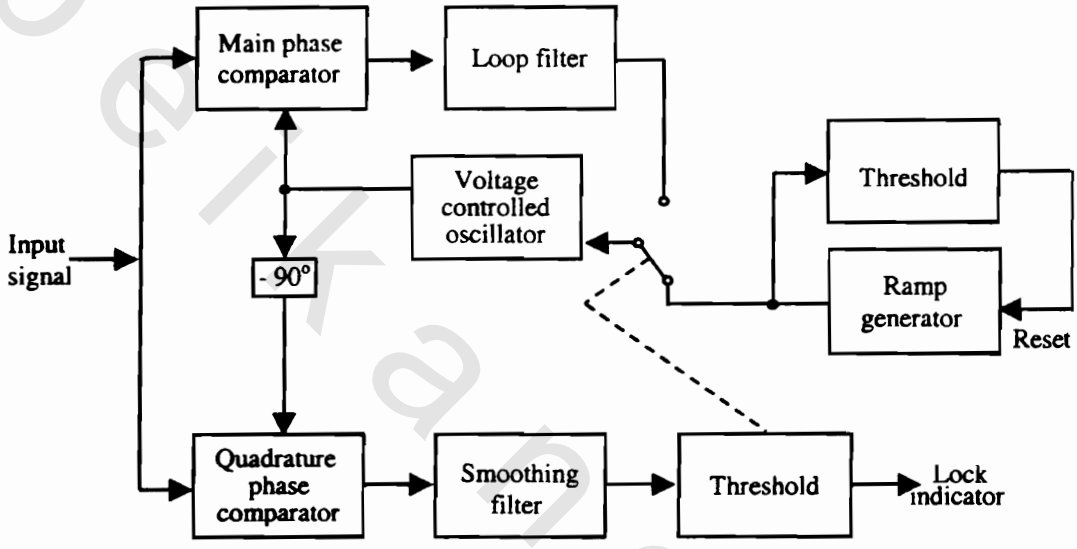
Fig. 11.18 Digital phase frequency detector

a) circuit b) waveforms

c) outputs at Q_A and $\overline{Q_B}$ d) average output voltage

Problems:

1- Discuss how the PLL sweep acquisition system shown works. Obtain various signals, and show how this circuit can be used as the basis for a spectrum analyzer.
Hint: The locked condition can be sensed by the threshold circuit which then disconnects the frequency sweep and connects the PLL for normal operation.



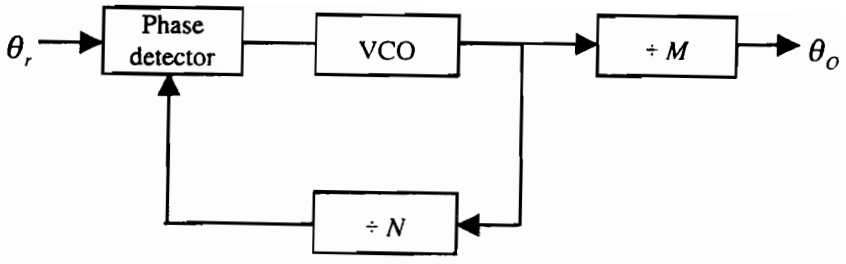
Prob. 11.1

2- Consider a DSBSC modulated system where a received signal is $m(t)\cos\omega_c t$, and the local carrier is $2\cos[(\omega_c + \Delta\omega)t + \delta]$, where $\Delta\omega$ and δ are the local carrier frequency and phase errors respectively. Discuss the effect on the output. When is the output truly the demodulated signal?

3- It is desired to design a frequency synchronizer to cover the frequency range from 100 to 109 MHZ in 1 MHz increments, and a reference frequency of 1 MHz is used. Design such a synchronizer.

4- A frequency synthesizer is to cover the frequency range from 10 to 10.1 MHz with 1 kHz resolution. The reference frequency is 100 kHz. Design the synthesizer. What is the VCO frequency? Consider using a post divider.

5- Show how a PLL may be used as a phase detector, and obtain the spectral response and bandwidth for a first order loop and for a second order loop.

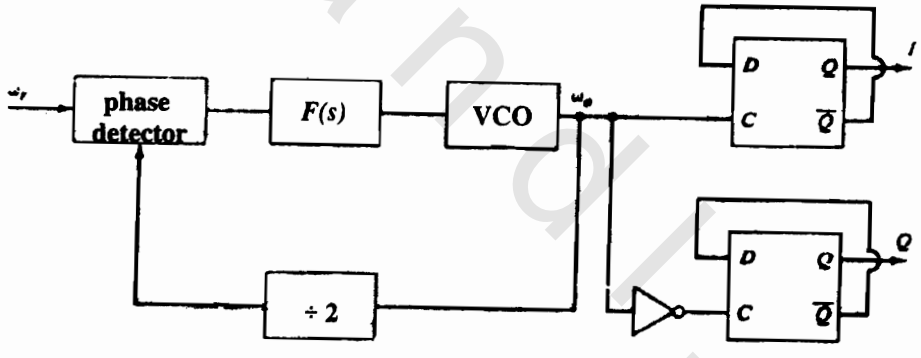


Prob. 11.4

6- Verify eqns. (11.31-11.33) for the frequency synthesizer, and obtain the rise time and the 3dB point. Take $k_V = 10\pi \ rad/s$.

7- Analyze the frequency synthesizer of a second order loop, when a zero is added. Discuss the result.

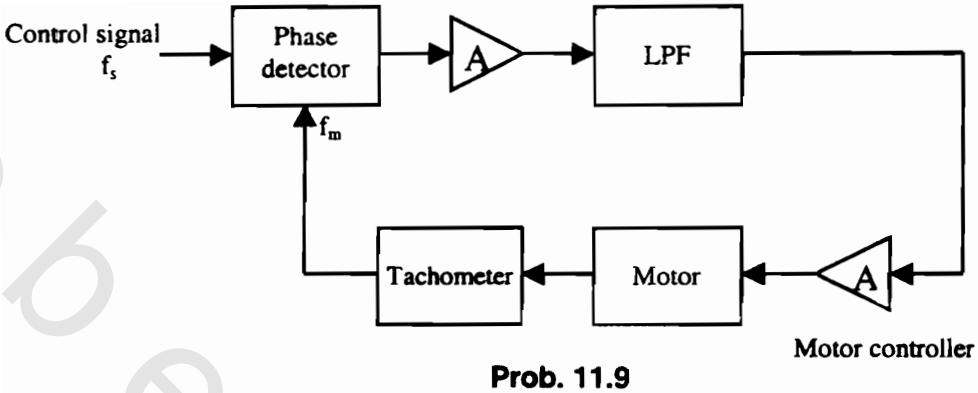
8- The circuit shown represents one method of obtaining a signal together with the signal shifted in phase by 90°. Sketch the timing diagram and explain how the circuit works.



Prob. 11.8

9- The figure shows a PLL motor speed control circuit. In this case, the PLL is an electromechanical feedback loop, and the tachometer output is a voltage waveform with a frequency that is proportional to the motor speed. Show what happens under lock-in condition, and how the motor speed may by contolled.

10- Analyze the transient response of
a) PLL b) frequency synthesizer.
Assume a small signal condition. Ignore the time response of the LPF, yet you may ignore the sum frequency components and the interfering signals.



Prob. 11.9

References:

1- "Telecommunication Circuits and Technology" A. Levin, Butterworth Heinman, Oxford, UK, 2000.

2- "Design and Applications of Analog integrated Circuits", S. Soclof, Prentice Hall, Englewoed Cliffs, N.J., 1991.

3- "Modern Communication Circuits", J. Smith, McGraw Hill, N.Y., 1986.

4- "Designer's Handbook of Integrated Circuits", A. Williams, Mc-Graw Hill, N.Y., 1986.

5- "Television Electronics", M. Kiver, M. Kaufman, Van Nostrand, Reinhold, N.Y., 1983.

6- "Introduction to Communication Systems", 2nd ed. F.G. Stremler, Addison Wesley, Reading, Massachusetts, 1982.

7- "Linear Integrated Circuits", J. Mc Menamin, Prentice Hall, Englewood Cliffs, N.J., 1985.