CHAPTER 15
TV (Video) Camera

15.1 The Vidicon Camera:

Although electronic imaging tubes such as vidicon are not of much use any more, they are easier to understand, and thus, we start with the vidicon camera tube. It consists of a cylindrical glass envelope containing an electron gun at one end and a target and a faceplate at the other. The tube is surrounded by a yoke containing electromagnetic focus and beam deflection coils. The faceplate is coated on the inside by a photoconductive layer over a thin metallic film (Fig. 15.1). This thin metallic film does not hinder light from passing through. This double layer forms the target. A small positive voltage is applied to the metal coating of the target.

Behind the target is a positively charged fine wire mesh. In the dark, electrons from the electron gun passing through the mesh decelerate as they deposit on the inner surface of the photoconductive layer of the target with almost zero velocities. Thus, a supply of negative charges is available on the inner side of the photoconductive material. As electrons deposit on the inner surface of the photoconductor, a positive charge builds up on the thin metallic film. Thus, the photoconductive layer behaves in the dark as a capacitor with very high internal resistance, not allowing electrons to flow through to the positive film. The voltage drop across the capacitor is $\frac{\Delta Q}{C}$, where ΔQ is the charge accumulated on either side of the capacitor. The voltage on the inner surface is $V_B - \Delta V$, where V_B is the positive voltage on the thin metallic film and is in the order of $10\,\text{V}$. In the dark, this voltage drop is uniform. Each cell on the photoconductor is not just a capacitor, but it is a combination of a capacitor and a resistor. The resistance in the dark is nearly 20 MΩ. Due to the continuous supply of decelerated electrons with zero velocities (due to the decelerating grid), the voltage on the electron beam side falls to $6V\,(\Delta V = 4V)$, and remains constant in the dark.

To utilize the property of photoconductivity, an electric field must be impressed across the photoconductor. In order to develop a positive charge pattern - which is to be interrogated by an electron beam - a positive voltage is applied to the signal electrode. A negative voltage is established on the opposite side by an electron beam where electrons arrive at almost zero velocity and zero voltage (due to the decelerating mesh).

The surface on which the charges are to be stored must have high resistivity to prevent the charges from being lost laterally during storage. The, bulk resistance of the material must also be high enough to prevent the loss of the voltage across the thickness of the layer during the intervals between successive scans. The voltage that is applied across the photoconductor is called the target voltage. When light is absorbed in the photoconductor, the effective resistance decreases and current flows through the resistor, i.e., the resistor discharges the capacitor, and a more positive voltage appears on the storage surface when light is observed than in the dark. The positive voltages that are built up on this surface are proportional to the illumination at each point at the image.

We may also say that electrons and holes generated optically in the photoconductor are separated by the electric field, such that electrons move to the positive electrode, and holes move to the negative surface. The positive charges that are stored on the storage surface constitute the charge image.

Now we assume - in the presence of bright light - that the resistance decreases to 2MΩ. The change in resistance is sharply localized in individual cells. Thus, a picture of various luminance levels is painted on the photoconductive material as regions of various resistances or leakages. Thus, the variation in the luminance is translated into a resistance pattern, and hence a voltage pattern. In this example, the voltage varies from 6V for black to 9.5V for maximum illumination (Fig 15.2). Alternatively, we may say that the light pattern is painted into a charge pattern, i.e., static negative charges (electrons from previous scans) will be present in dark areas and absent in light areas on the storage surface.

As the e-beam contacts the cell, it acts to form a closed path for current, with zero potential at some point behind the decelerating mesh. A charging current flows according to the circuit (Fig. 15.3). This charging current replenishes electrons lost, due to the discharge of the capacitor through the photoconductive resistance. In other words, due to light, electrons penetrate the photoconductive material due to the reduced resistance. The electron beam replaces those electrons, giving rise to current proportional to the local light intensity at that point. The video signal is represented by variations in this current.

We must note that in a storage type TV camera tube the signal is developed by an electron beam that scans the stored charge images that are produced by light (photo-generated charges) on the target, where low velocity scan is used. Low velocity scan does not pertain to the speed with which the beam progresses across the picture area of the target. Instead, the term indicates that the electrons in the beam are moving slowly as they approach the stored charges of the charge image. The purpose of the scanning electron beam is to deposit electrons on the positively charged area of the stored charge image, where photo-generated holes are accumulated, and where photovoltage corresponds to the brightness of the scene at that point. The use of a low velocity beam assures that most of the electrons of the beam will land on the stored charge, until its total voltage drops to near zero without emissions of secondary electrons.

The element of the storage target - being interrogated by the scanning beam - develops a positive voltage in the interval between successive scans of the spot, such that $C\Delta V = Q$. The scanning beam deposits electrons on this element, driving its voltage down to zero in the interval BC (Fig. 15.3a). It then continues to the next portion of the scan image, where the process is continued. The point that is just neutralized will start to charge positively again along the curve CD, if light is still present at that portion of the image.

At time t_2 - when that element is scanned again - that portion of the target capacitance will be recharged to its original voltage. We note that the stored charge image is a positive voltage with respect to the cathode of the electron beam. However, the positive image charge voltage is actually a result of discharging the target capacitance. The electron beam is, thus, dissipating this positive voltage and restoring it to zero volts. In actuality, it is recharging the target capacitance. We amplify the current that flows in the signal plate electrode of the target, and hence, obtain a television signal.

Fig. 15.3b illustrates what takes place in the time interval between scans of this point on the target. The photo-induced current is flowing through the resistance R_p, and the target capacitance C. No net charge is being added to the target assembly, nor does any of this current flow into or out of the signal plate at this time.

As the capacitor C is being partially discharged, it becomes more positive (less negative) on the second surface. In Fig. 15.3c, the scanning beam deposits electrons on the surface. This flow of electron current recharges the capacitor, and an equal current flows through the signal plate to the amplifier. In the absence of light, little or no build up of voltage occurs on the scan surface. Consequently, no current is developed when the beam scans that spot.

The current that flows out of the signal electrode always flows in the same direction, and is zero in the absence of light. There is zero dc component in the video signal current when no beam is landing on the target and the absolute level of the current flowing out of the signal plate relates directly to the voltage of the charge pattern that is being scanned by the electron beam.

Thus, we may say that the charging of the capacitor during the e-beam contact puts in enough charge to compensate for the charge lost in between scan lines within a frame, until the exact spot is sampled again.

Ex. 15.1:

Show that the charging current in each element of a vidicon is proportional to the voltage difference across the target element.

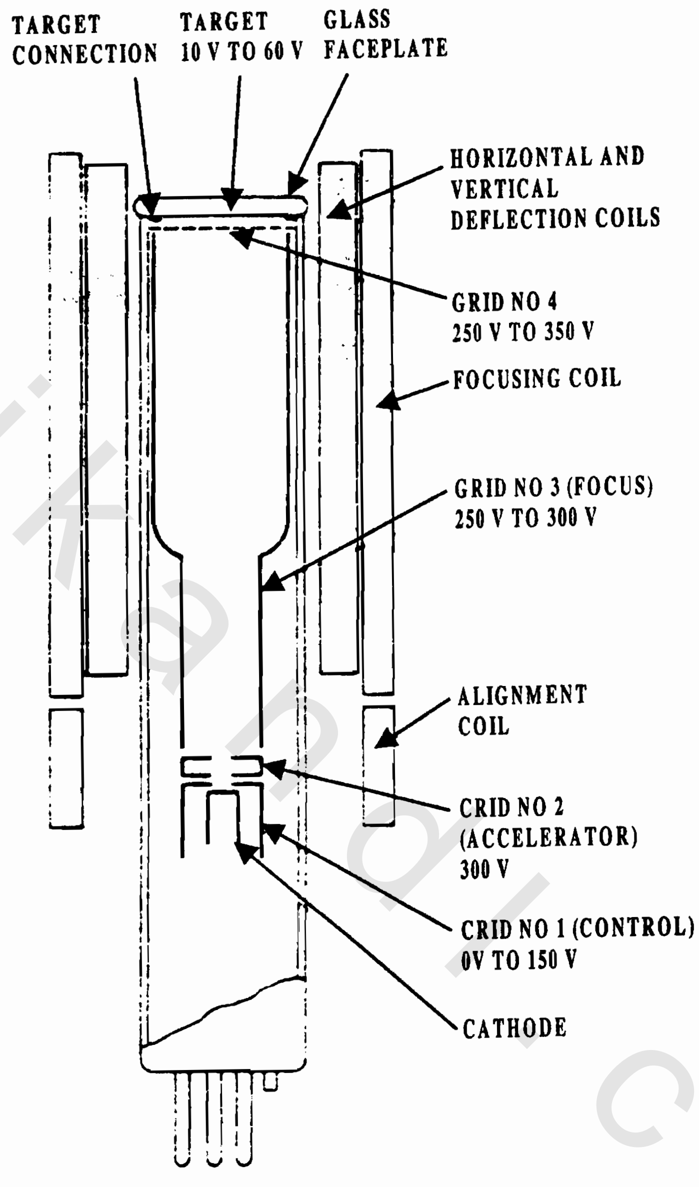


Fig. 15.1 Vidicon camera tube

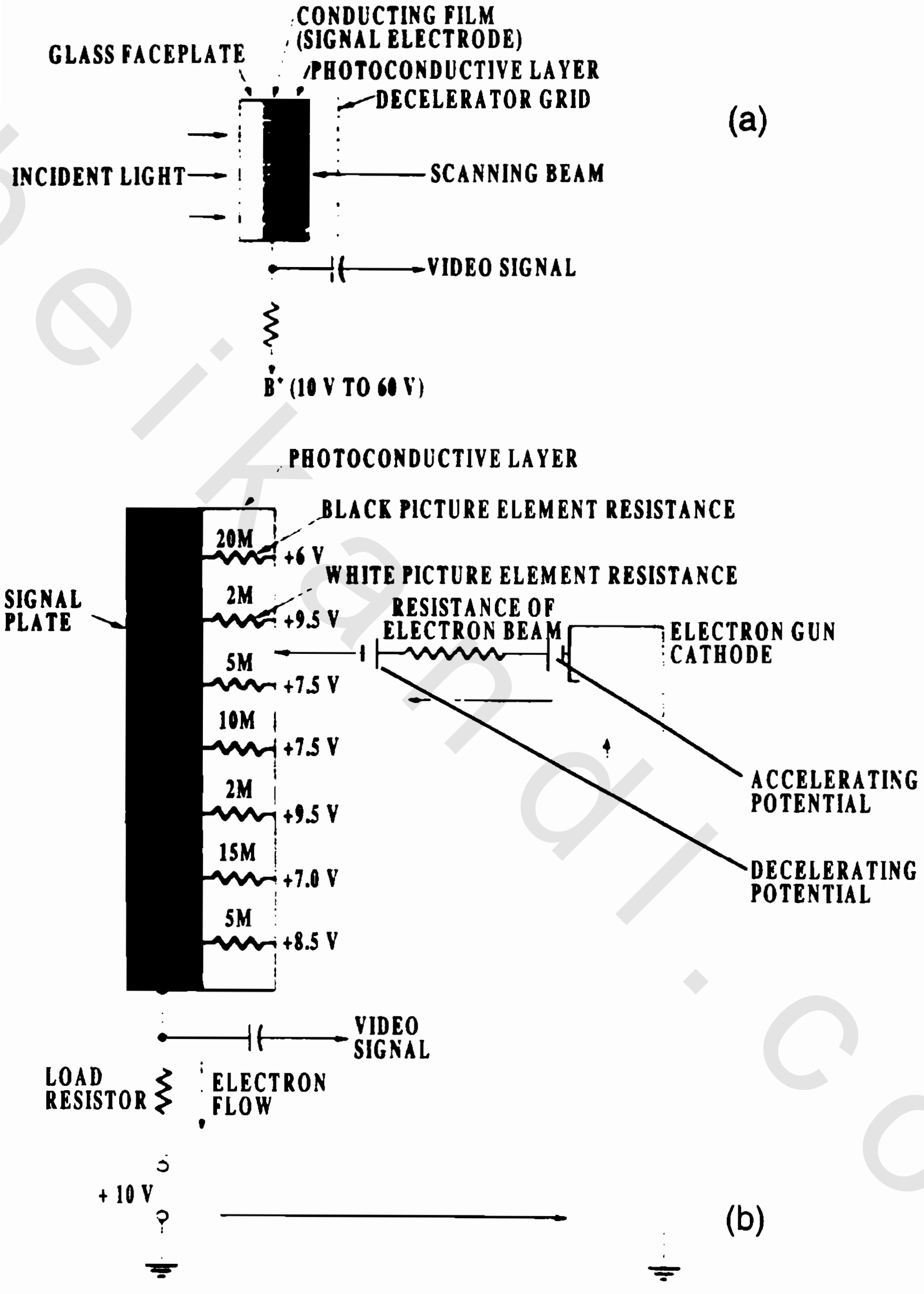


Fig. 15.2 Vidicon operation
a) layout b) voltage pattern

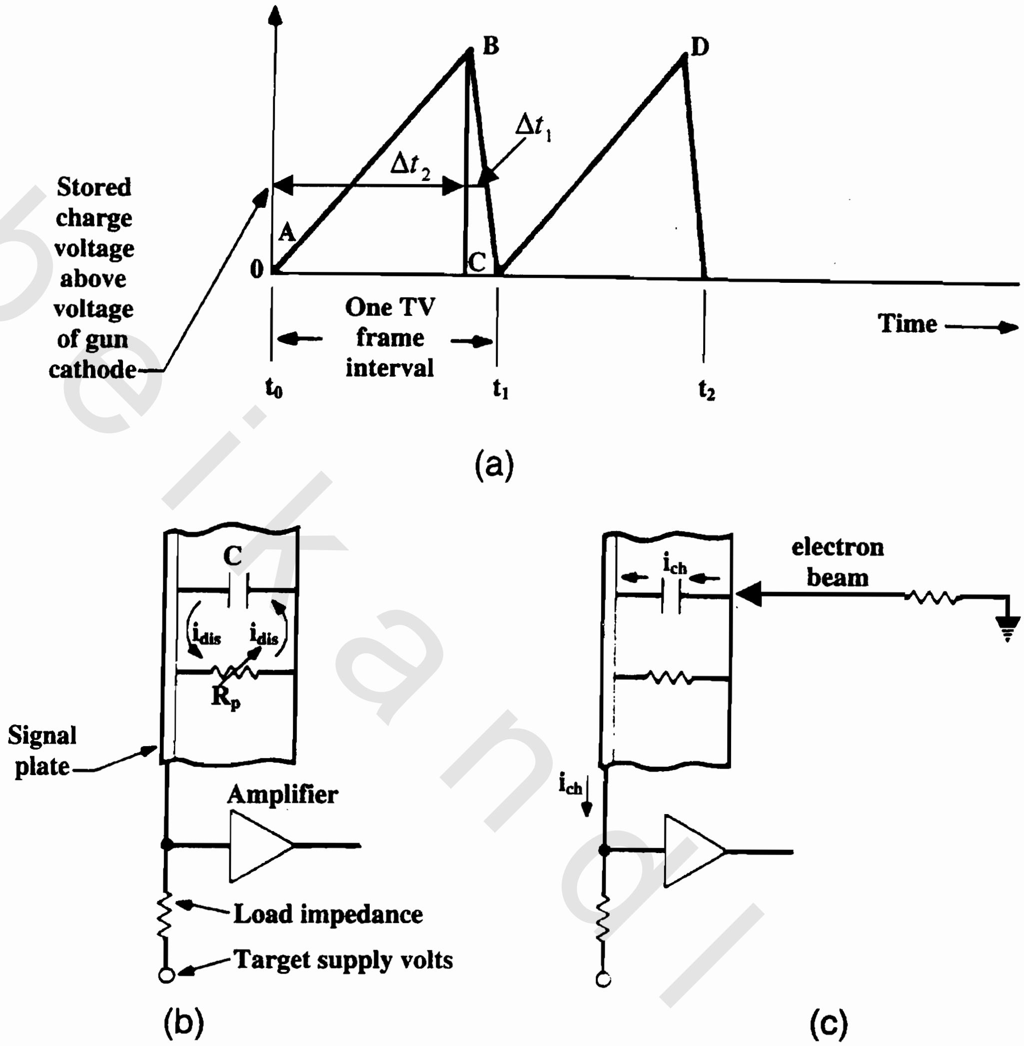


Fig 15.3 Equivalent circuit for vidicon operation

a) discharging and recharging of the capacitance of an elemental area on a storage type target.
b) current flowing in a photoconductive target elemental area while the target is integrating a charge.
c) current flow when a low velocity electron beam is interrogating the element.

Solution:

Since the e-beam contacts the pixel during the charge time, it is this charging current that flows in the load resistor, and is indicative of the original voltage decrement due to light ΔV (photovoltage) at that element, such that

$$\Delta Q_{gained} = \overline{i_{ch}} \times \Delta t_1, \qquad (15-1)$$

where $\overline{i_{Ch}}$ is the average charging current during contact time with the e-beam Δt_1. During leakage time Δt_2 (roughly the time between frames), the average current $\overline{i_{dis}}$ is determined by the equation.

$$\Delta Q_{lost} = \overline{i_{dis}} \times \Delta t_2 \qquad (15-2)$$

Assuming linearized exponentials during discharge,

$$\overline{i_{dis}} = \frac{\Delta V}{R_{Ph}} \qquad (15-3)$$

For charge balance, $\Delta Q_{gained} = \Delta Q_{lost}$

$$\overline{i_{ch}} = \frac{\Delta V}{R_{ph}} \frac{\Delta t_2}{\Delta t_1} \qquad (15-4)$$

Hence, the charging current is proportional to the photovoltage ΔV. It is this charging current that we sample in the load resistance. The e-beam scans the photoconductive layer in a standard 525 lines per frame. As the e-beam contacts each positively charged element, it gives up electrons in proportion to the voltage at that point.

A varying electron current is produced, which flows in the load resistor, producing a video signal. Note that the function of the e-beam is just to read out the information of the scene already stored as a voltage pattern or a static charge pattern.

We must note that the e-beam pumps in - upon contact with an element - an amount of charge equal to that lost due to the discharge of the capacitor through the leakage resistor (photoresistance), until the next frame for the same scan position. In other words, for a scene that does not change fast from frame to frame, we have a situation of steady state balance between the discharging action and the charging for each element. This charge current is proportional to the charge lost due to leakage, and hence, proportional to the voltage pattern. We detect this charging current during the time of contact as load current. Output video signal is the variation of this charging current from element to element. Once the video signal is obtained, the sync and blanking pulses are then added to obtain the composite video signal (Fig. 15.4), so that it becomes ready for transmission (Fig. 15.5).

15.2 Charge Coupled Devices (CCD):

Charge coupled devices (CCDs) are dynamic devices that move charge along a predetermined path under the control of clock pulses. Fig. 15.6 shows an MOS capacitor on a p-type substrate. With a large positive gate pulse applied, a depletion region exists under the gate.

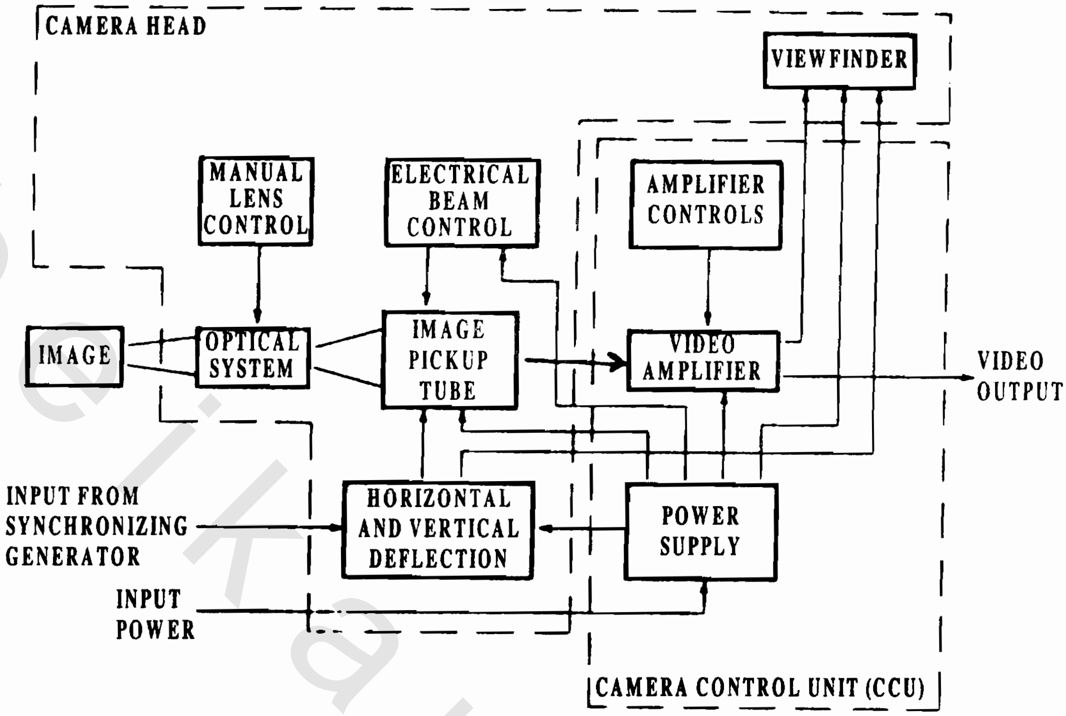


Fig. 15.4 A simplified diagram of a typical monochrome TV camera

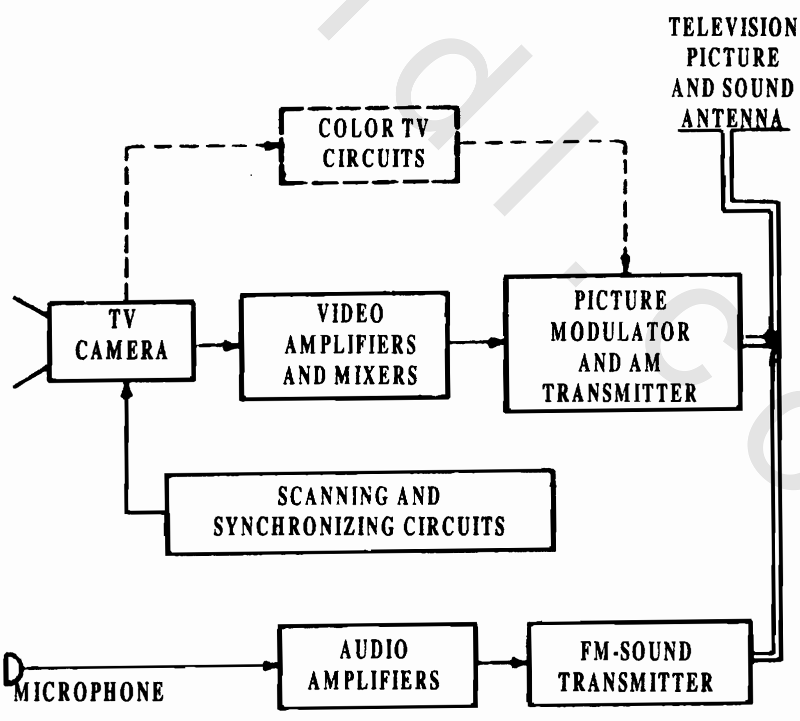


Fig. 15.5 A simplified block diagram of a TV transmitter

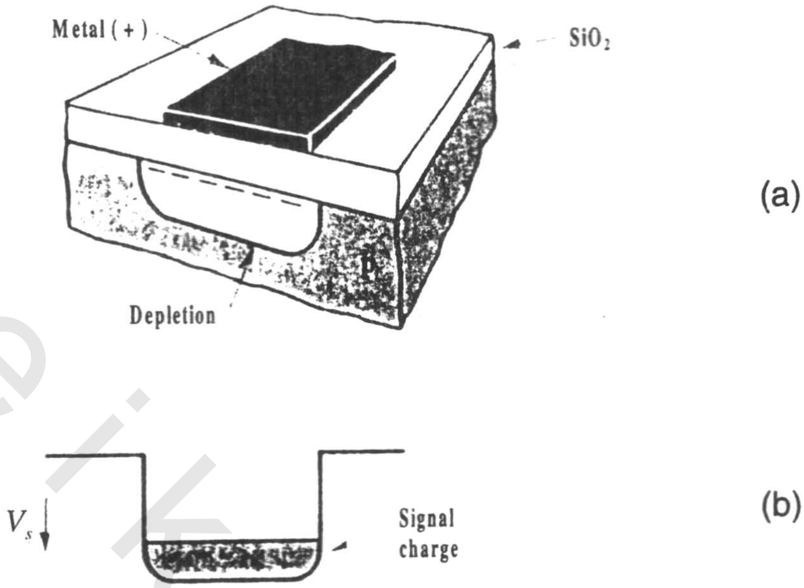


Fig. 15.6 MOS capacitor with a positive gate pulse

a) depletion region and surface charge
b) potential well at an interface partially filled with electrons corresponding to surface charge shown in (a)

The surface potential forms a potential well, which can be used for the storage of charge. If the positive gate bias has been applied for a sufficiently long time, electrons accumulate at the surface, and a steady state inversion layer is formed. The source of these carriers is the thermal generation of electrons at or near the surface. The inversion charge sets the limit for storing charge. The time required to fill the well thermally is called the thermal relaxation time. It is recommended that this time be much longer than the charge storage times involved in CCD operation. If instead of a steady state bias, we apply a large positive pulse to the MOS gate electrode, a deep potential well is first created. Before inversion has occurred by thermal generation, the depletion width is greater than that at equilibrium. This transient condition is called deep depletion. If we inject electrons into this potential well - electrically or optically - they will be stored there.

This storage is temporary, since we must move these electrons out, before thermal generation takes over. We must note that the deep potential well does not mean that electrons will stay far from the surface and deep into the bulk. On the contrary, electrons will be close to the surface. These electrons must be allowed to flow from one potential well to another quickly and without loss, and can be made to be injected, shifted and collected in packets.

The original CCD structure - proposed in 1969 by Boyle and Smith - consisted of a series of metal electrodes forming an array of MOS capacitors (Fig. 15.7). Voltage pulses are supplied in three lines L_1, L_2, L_3, each connected to every third electrode in the row G_1, G_2, G_3. These voltages are clocked to provide potential wells, which vary with time. At instant of time t_1, a potential well exists under each G_1 electrode, and we assume that this well contains a packet of electrons from a previous operation. At time t_2, a potential is applied also to the adjacent electrode G_2, and the charge equalizes across the common G_1 G_2 well, very much similar to a fluid equalizing its level in an expanding container. At t_3, V_1 is reduced, thus, decreasing the potential well under G_1. Now the charge flows into the G_2 well. This process is completed at t_4, when $V_1 = 0$. The packet, thus, has moved from under G_1 to under G_2, and the process repeats.

As this procedure is continued, the charge is next passed to the G_3 position, and so on until the end of the line. An input diode may be used to inject the charge and an output diode may be used at the end of the line to detect it out.

The three - phase CCD shown can be replaced by a two - phase structure (Fig. 15.8), in which voltages are sequentially applied to alternating gate electrodes from two lines. A two-level poly-Si gate structure is used, in which the gate electrodes overlap - a donor implant near the Si surface creates a built-in well under half of each electrode. When both gates are turned OFF, potential wells exist only under the implanted regions, and charge can be stored in any of these wells (Fig. 15.8b). With electrode G_2 pulsed positively, the charge packet shown is transferred to the deepest well under G_2 which is its implanted region (Fig. 15.8c). Then, with both gates OFF, the wells appear as in (Fig. 15.8b), except that the charge is now under G_2 electrode.

When we pulse G_1 positively, the charge moves to the implanted region under the G_1 electrode to the right. As excepted, CCDs have many applications such as delay, filtering and multiplexing signals. They are used as shift registers, digital memories and logic arrays.

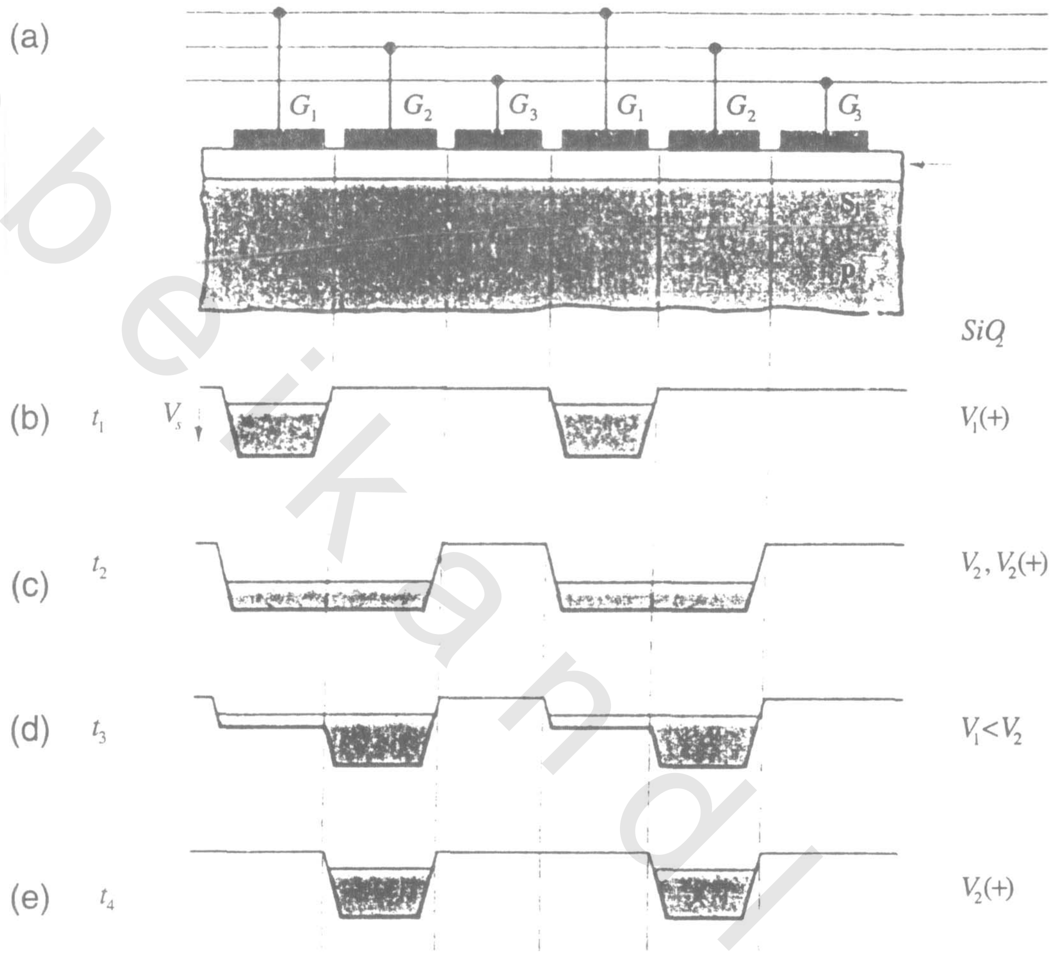


Fig. 15.7 Charge transfer for 3- phase CCD

a) layout

b) at $t = t_1$, G_1 electrodes are positive

c) at $t = t_2$, both G_1 and G_2 are positive

d) at $t = t_3$, potential on G_1 is reduced and charge flows to the second well

e) at $t = t_4$, the transfer of charge to the G_2 well is complete

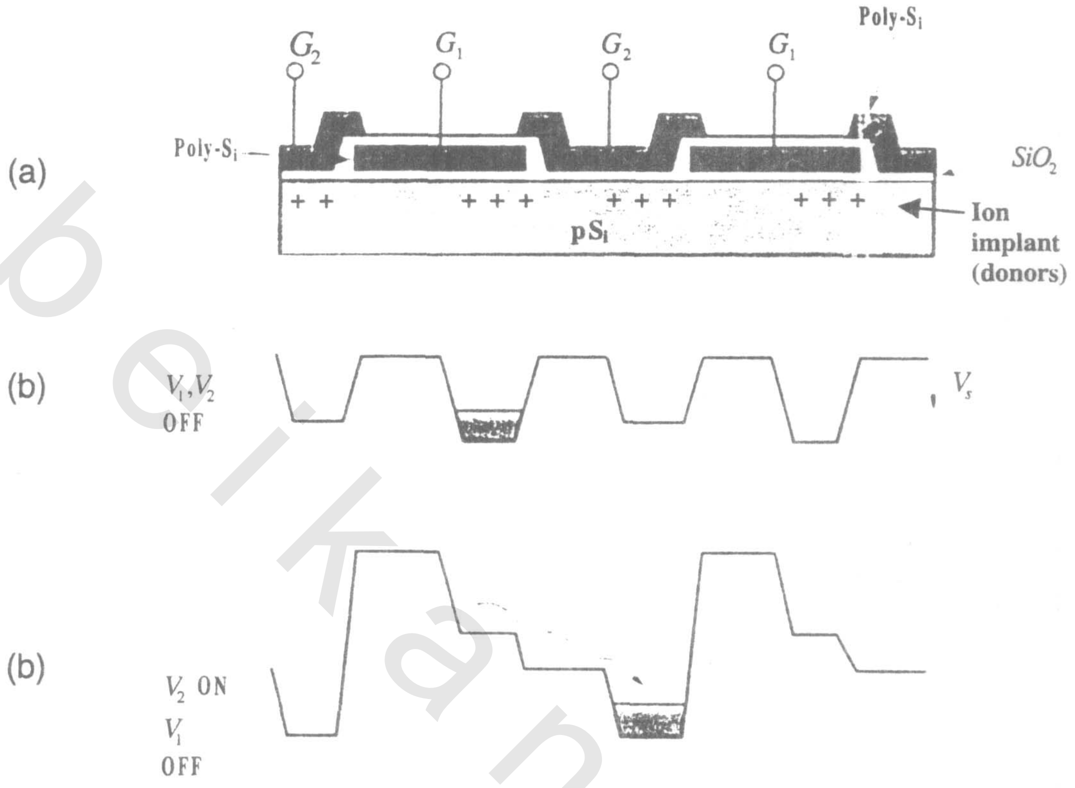


Fig. 15.8 Charge transfer for a 2 - phase CCD

a) layout b) V_1, V_2 OFF c) V_2 ON, V_1 OFF

A relevant application here is in imaging. An array of photosensors is used to form charge packets proportional to light intensity. These packets are shifted to a detector point for readout. There are two ways for accomplishing this in CCDs. One is the use of a linear array or line scanner. The scanner is moved relative to the image to complete the scan. The second method is the use of an area image scan, where the image is scanned electronically in both dimensions. The latter device can be used as an alternative to the electron beam in a TV imaging tube. Photons entering the silicon substrate-either through or between the electrodes - generate electron-hole pairs (photoconductivity).

The minority carriers (electrons) generated within the depletion regions - or within a minority carrier diffusion length of the depletion regions - are collected in the potential wells due to the electrode potentials. The number of electrons collected under a given electrode - within a given period of time (called integration time) - is proportional to the local light intensity. Thus, the pattern of charge that collects under the electrodes is a replica of the light intensity across the original image. Fig. 15.9 shows the single output pulse from imaging a light spot. At the end of the readout period, the device is switched to the integration mode and the cycle is repeated.

(a)

(b)

(c)

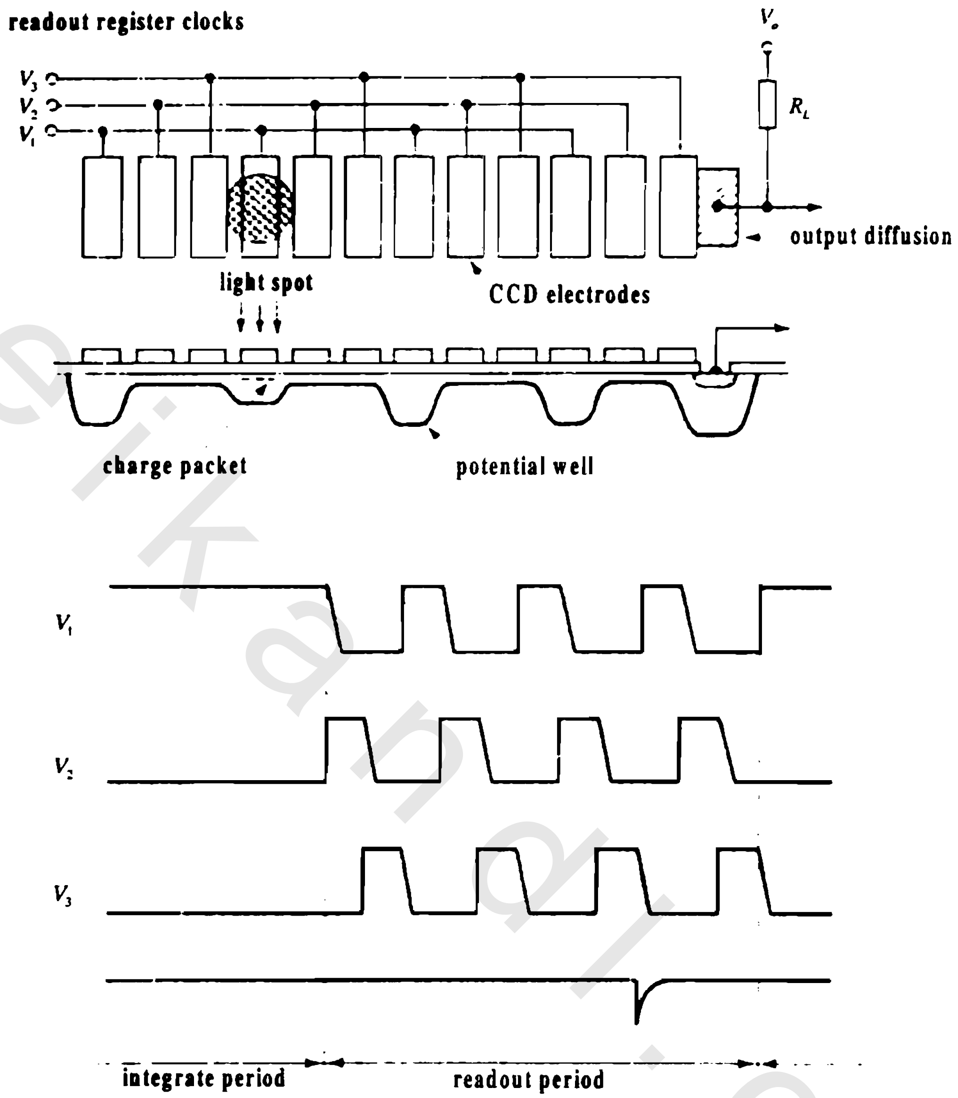


Fig. 15.9 Basic operation of a CCD imager
a) layout
b) potential well distribution
c) timing diagram for a 3-phase CCD

15.3 Solid State (CCD) Imagers:

Tube imagers served for the first 40 years of TV, but have ultimately given way to solid state (or CCD) imagers. Instead of an electron beam scanning out the stored image, an array of CCD's will have clock pulses drive out the charge in a two-dimensional scanning mechanism. The CCD imager performs three functions; photodetection, storage and scanning. There are many advantages for using solid state imagers over tube imagers. Among them of course is the low power, small size, light weight, long operating life, better sensitivity, electrical and mechanical stability and the elimination of field adjustment. CCDs have helped produce home use video cameras or camcorders.

The basic unit of a solid state imager is the CCD described before with the conducting electrode made from polysilicon, which is a transparent highly conducting type of silicon. Thus, light is not obstructed from reaching the depletion region. Fig. 15.10 shows two complete MOS capacitor imaging cells adapted for 3-phase transfer clocks. There are three separate electrodes for each cell, with one transfer clock phase connected to each of them.

During the charge integration period - which is the period for the build up of the stored charge image - one of the clocks V_2 is held high and the other two clocks low. Thus, there is a depletion region under the electrode connected to V_1, and the free electrons created by the optical input are collected in that region. The holes of course are recombined with electrons drawn out of the positive metal electrodes. Thus, the region under the V_2 electrode will collect the charge created under all three electrodes of that pixel. When transfer starts, the V_3 clock is made high and the V_2 clock voltage is slowly reduced. The result is that the charge under V_2 moves to be under V_3. At the end of the first part of the transfer, V_2 reaches zero and the charge is now fully under the V_3 electrode. Transfers take place simultaneously in every pixel that is connected to the same three clocks. At the end of one full cycle, the charge from the first pixel is now under V_2 of the second pixel. Thousands of transfers may be carried out with speeds up to tens of MHz with negligible loss of charge.

In the architecture of a practical imager, channel stops (or barriers) are built to constrain the charge from spreading into the wrong direction, e.g., vertical instead of horizontal. Overflow drains are also introduced to prevent filled wells from spilling over and smearing the image.

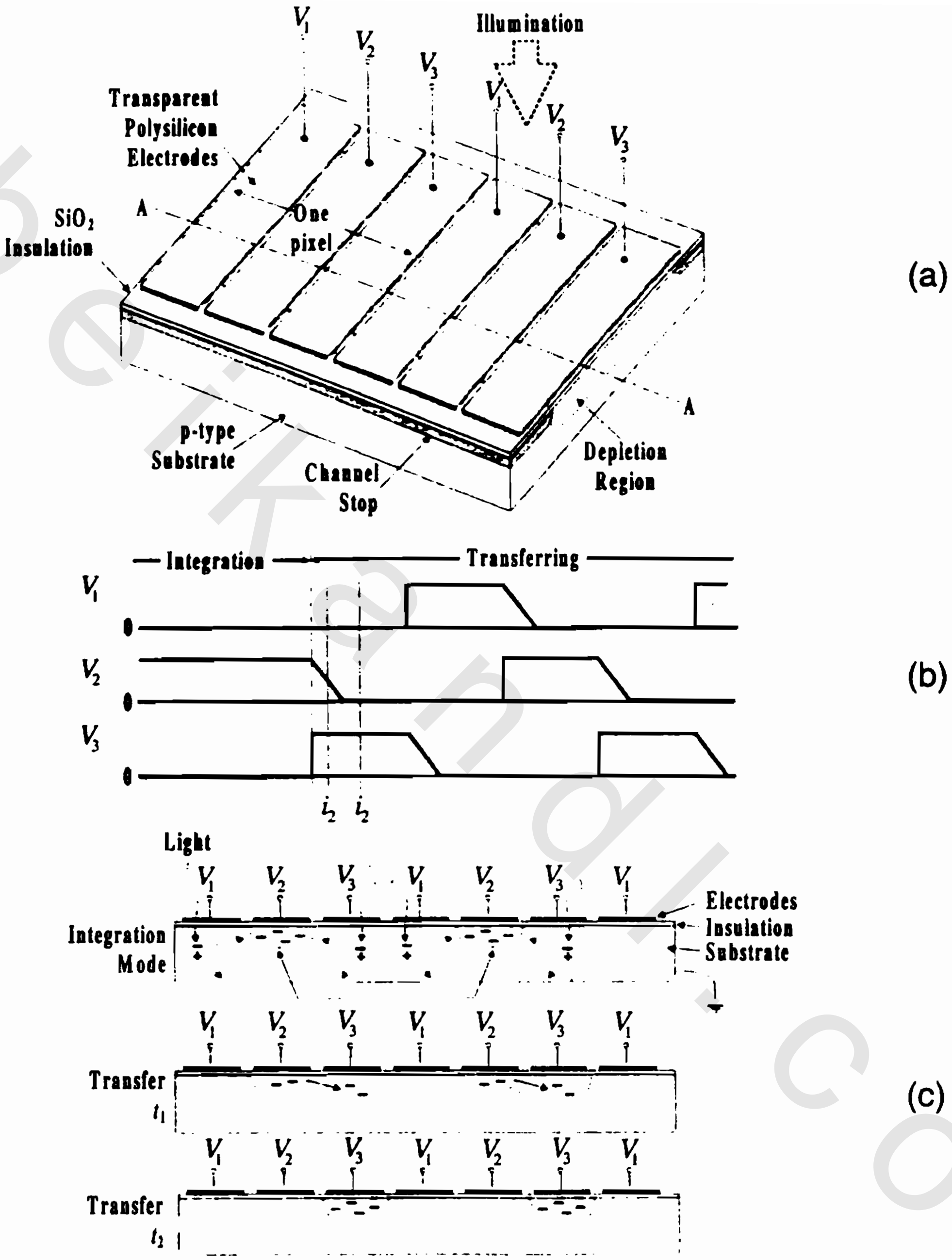


Fig 15.10 Charge coupling in a CCD imager

a) layout
b) timing diagram
c) charge transfer operation

There are three basic CCD architectures. The simplest is the frame transfer (FT) (Fig. 15.11). In this architecture, there are two complete arrays of cells, each containing all the pixels of the image. One array receives the optical image, and thus, performs the integration. The cells of this array are designed to shift vertically. During the vertical blanking interval (VBI), the entire image charge is shifted as rapidly as possible into a second array which is masked from light by an opaque coating. This transfer process clears the pixels of the imaging array, so a new integration period can start. During the horizontal blanking intervals (HBI) of the next vertical scan, this second array is transferred down one line at a time into a readout register. During active horizontal line scan, the readout register is clocked to transfer the charge representing the pixels horizontally into an output gate, where they are converted into a composite video signal.

We should note that the FT configuration requires the optical image on the imaging area to be rotated 180°, as it is when imaged by a single lens. Pixels of the lowest right corner of the image are the first to be clocked out. We must note also that charge integration occurs continuously in the pixels as long as light is on the array. Integration continues during vertical blanking, i.e., during vertical transfer. Since the charge image is moving during the transfer, the charge created during this time will be smeared vertically.

An alternative configuration - called interline transfer (IT) CCD- avoids largely the smear problem. In this architecture, the imaging and storage arrays are interleaved (Fig. 15.12). Each pixel in an IT image has two CCD cells side by side. One cell performs integration and the second cell - which is masked from light - is the vertical transfer shift register. During vertical blanking interval, all the charge collected in the integration cells of all pixels is shifted horizontally into the adjacent vertical shift register cells in one massive single transfer. Then, the vertical shift registers are clocked down one line at a time and read out, the same way as in FT device. Since the optically masked vertical shift registers are within the image area, there is loss of light energy because of the masks, i.e., there is a 50% loss of sensitivity. Small lenses may be used to direct all of the incident light into the imaging cell. This is called on-chip lens. Since the horizontal transfer to the vertical shift registers has only a single chip, there is no possibility of smearing. However, a different type of smear may occur as light may leak around the masks, or long wavelength light may penetrate deeply into the substrate, generating charges that may migrate into the vertical shift register. This is called vertical smear.

The small transfer smear problem of the IT imager can be further reduced by the frame interline transfer (FIT) CCD structure, which combines the concepts of FT and IT structures (Fig. 15.13). The operation is the same as IT imager during the integration period, but all pixels are moved to their vertical shift registers at the start of the vertical blanking interval, then shifted down into the optically masked storage register.

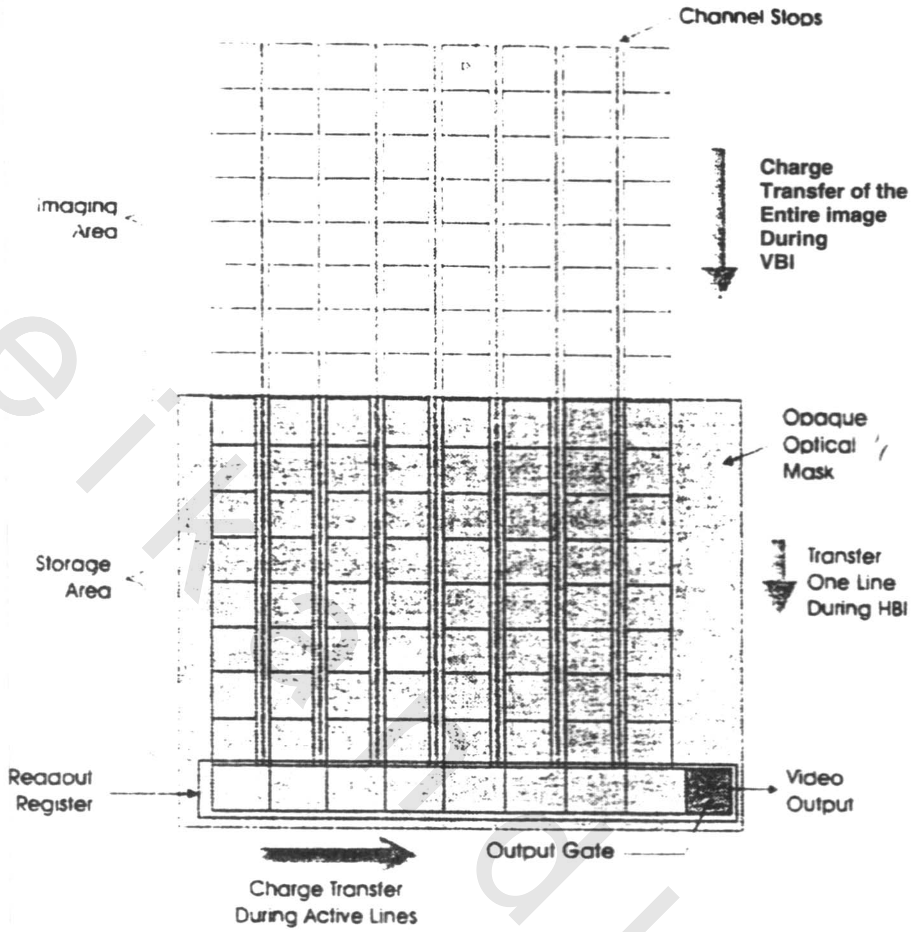


Fig. 15.11 Frame-transfer (FT) CCD architecture

These transfers happen at 60 times the line scanning rate, thus, reducing vertical smear. During active scanning time, lines are shifted into the readout register as in FT imager. Interlacing can be achieved by combining the output of vertically adjacent pixels on each field (Fig. 14.14).

15.4 CCD performance:

The first performance parameter is resolution. Resolution is determined largely by the number of pixels in the CCD camera, as well as the resolution of the optics used in the camera system. The number of pixels across the imager determines the horizontal resolution. Vertical resolution is determined by the number of pixels in the vertical direction, and is given by the number of active lines.

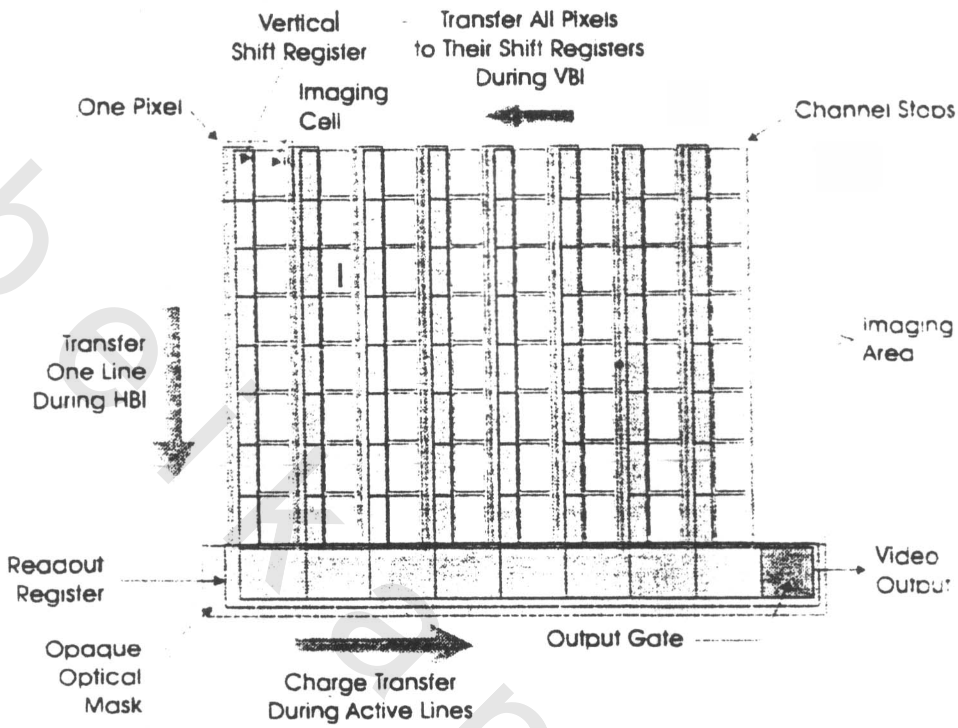


Fig. 15.12 Interline-transfer (IT) CCD architecture

The sensitivity of a CCD depends on the percentage of a pixel's area that is sensitive as well as the optical and quantum efficiencies. High sensitivity is desirable to allow shooting under low light conditions.

Noise is another serious consideration for CCD. One source of noise is the dark current. Dark current can fill the wells with thermal electrons before the photoelectrons have a chance to build up. This dark current may vary from pixel to pixel, and appears as a random noise with pixel to pixel variation appearing as a fixed pattern. Another source of noise is the photon (quantum) noise, and is due to the quantum nature of light.

Ex. 15.2:

What is the photon noise for 100 photons/pixel/second illumination?

Solution:

If a CCD is illuminated with 100 photons / pixel / second on the average, the actual number of photons striking any particular pixel in one second will be a random number. Statistically that number has a Poisson distribution, so its standard deviation is equal to the square root of its mean.

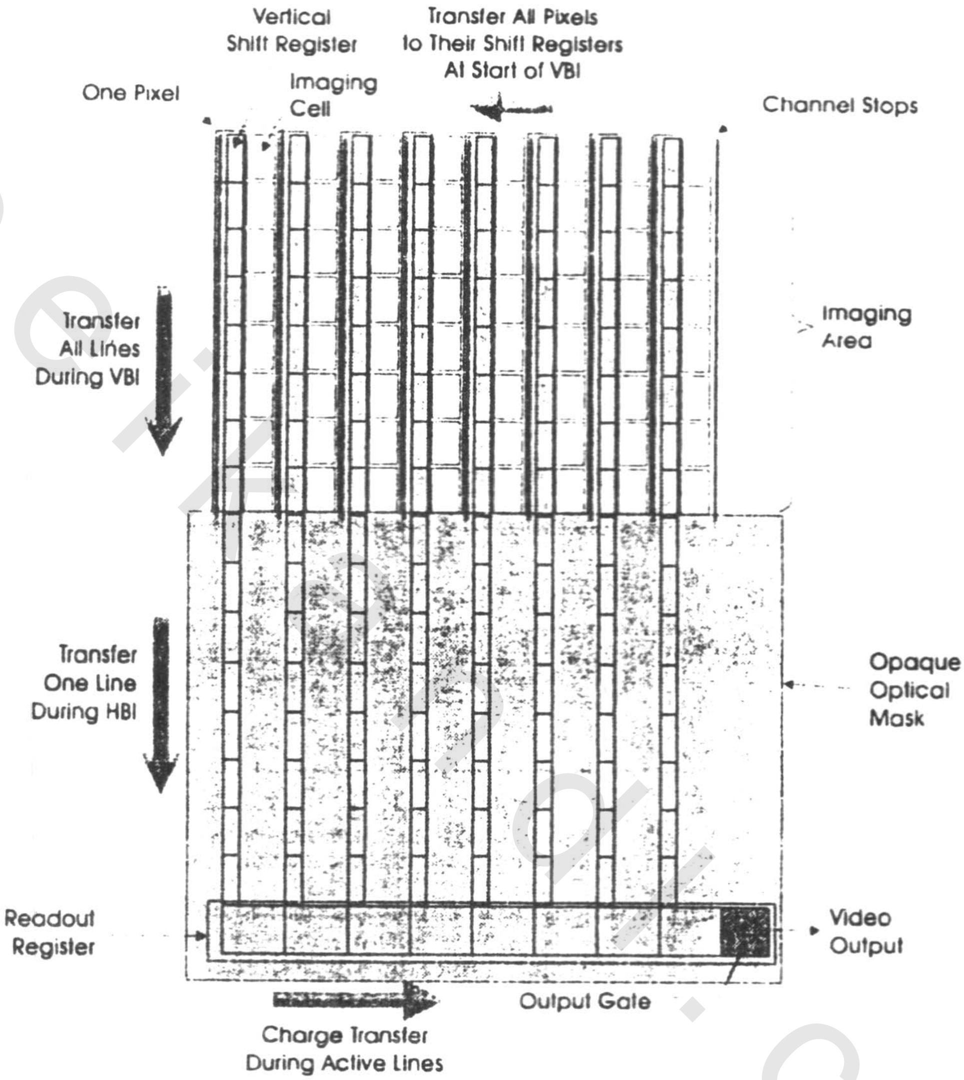


Fig. 15.13 Frame - interline - transfer (FIT) CCD architecture

The average number of photons incident upon pixels would be 100, with a standard deviation of 10. In general, the photon noise component is the square root of the number of electrons that accumulate in a well (photoelectrons plus thermal electrons). This is the dominant noise under high exposure or high dark current condition. On the other hand, readout noise due to on-chip electronics becomes the dominant noise factor under short exposure low light conditions, where the dark current and photon noise components are small.

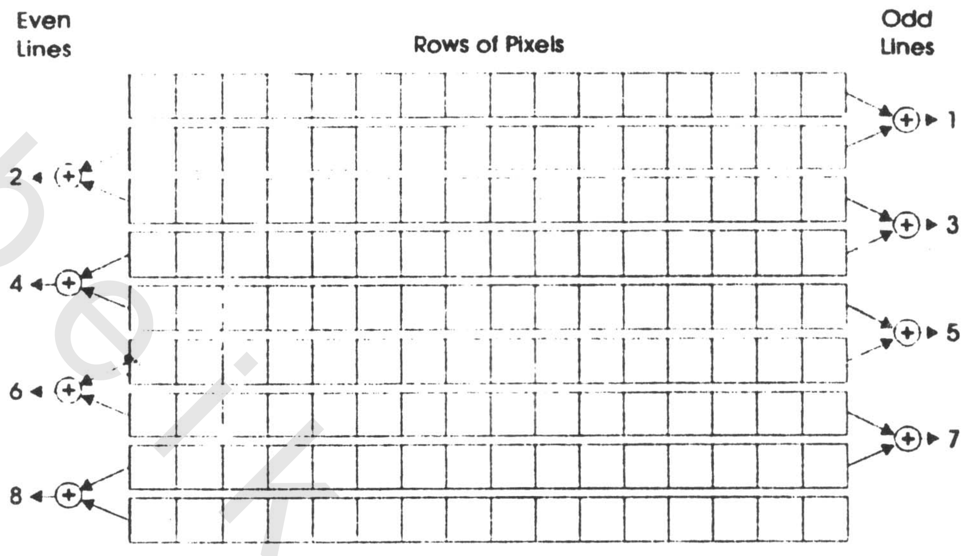


Fig. 15.14 Interlacing of an IT or FIT CCD by combining adjacent lines

Also, overexposure of a CCD sensor can cause blooming of the image, as excess photoelectrons spread to adjacent pixels. Defects in the crystal lattice can cause a dead pixel, which will not hold photoelectrons. Since charge is shifted through the pixels on its way out of the chip, one dead pixel can wipe out all or part of an entire column.

Since the charge developed in a pixel must be shifted from well to well - as many as a thousand times or more before leaving the chip - this requires the charge transfer efficiency to be extremely high, or significant numbers of photoelectrons will be lost in the readout process.

15.5 Color Reproduction:

A single transfer imager is suited to monochrome cameras. In camcorders, the line transfer imager is more commonly used, while, FIT is used for broadcast type CCDs cameras. A typical CCD solid state pick up unit for portable cameras and camcorders using FT has some 300000 pixels on a small rectangular substrate. There are in excess of 500 vertical shift registers, one horizontal shift register and accompanying pulse control circuits all on the same chip.

The scene that is recorded by the camcorder is inverted through the lens, and when it is displayed on the surface of the imager, it is an inverted mirror image (Fig. 15.15). Scanning of the pixels in the imager starts at the lower hand corner, and finishes at the top left hand corner. The horizontal shift register is at the bottom of the stack. It is there so that the first pixel to be readout is the one at the start position in the lower right hand corner.

For color reproduction, the light sensitive cells are covered by an array of green, cyan, magenta and yellow filters (Fig. 15.16). The light transfer characteristics of these complementary colors are better than the primary colors. (Fig. 15.16c).

The luminance signal is obtained by adding two adjacent cell pairs and color differences are obtained by adding two adjacent cell pairs, then subtracting the cell pair values. Each readout line provides one color difference signal, the other color difference comes out as the next line (Fig. 15.16b). This situation of color matrix describes portable CCD cameras and camcorders.

In more sophisticated systems (broadcast type), there are three imagers and light splitting optics. There are three separate imagers R, G, B mounted and sealed as a prism block. This arrangement (triple imager) is too expensive for the consumer market.

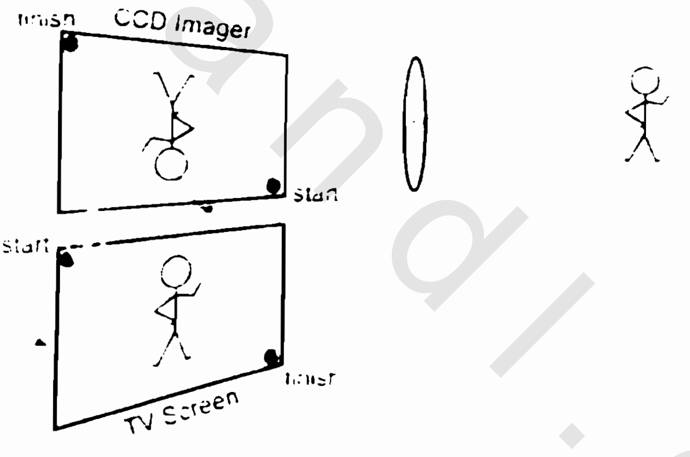
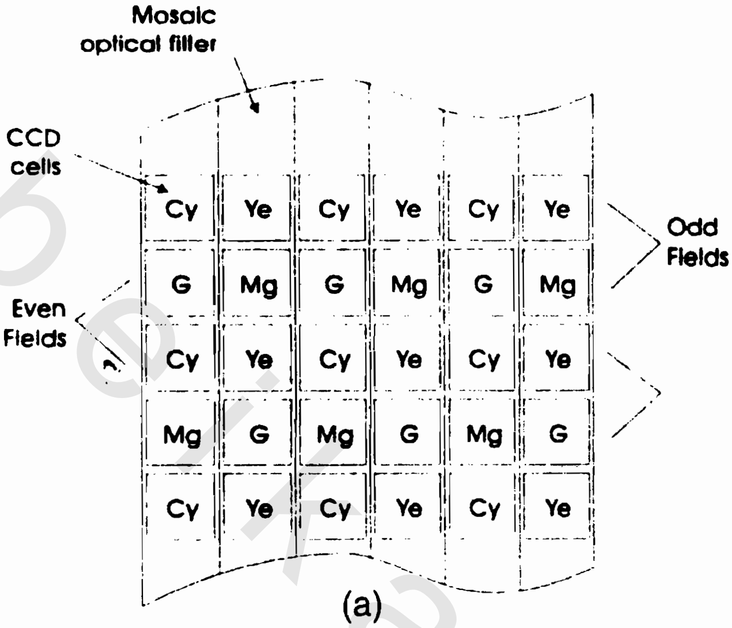


Fig. 15.15 Inverting an image of a scene in a CCD

The objective of color light splitting is to separate the color components. A dichroic mirror is the key to such splitting. It allows certain wavelengths to pass through, and other wavelengths to be reflected without any absorption of light. A dichroic mirror (Fig.15.17) consists of one or more thin coatings on an optical substrate (glass). The coatings have different refractive indices from the glass and precise thicknesses. Interference between the light waves reflected or refracted at each surface in the filter causes a wavelength dependent behavior (Fig. 15.17b).



(a)

First Line

$$Y = \frac{(G + Cy) + (Mg + Ye)}{2}$$

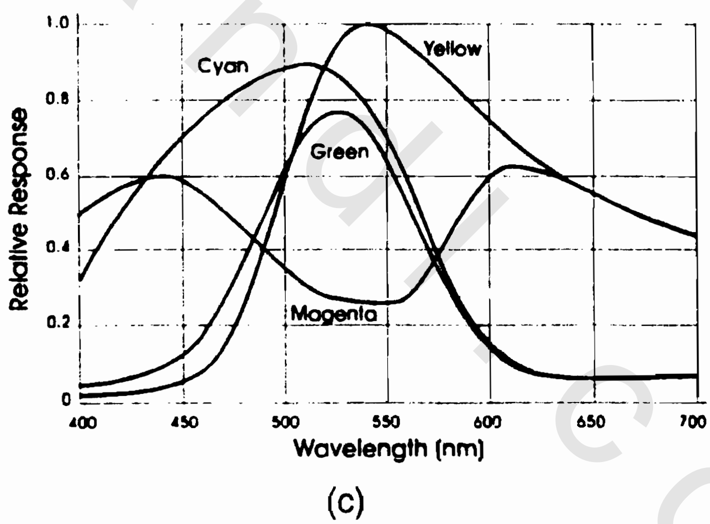
$$R - Y = (Mg + Ye) - (G + Cy)$$

Second Line

$$Y = \frac{(G + Ye) + (Mg + Cy)}{2}$$

$$B - Y = (Mg + Cy) - (G + Ye)$$

(b)



(c)

Fig. 15.16 Color CCD using complementary color filtering

a) cell layout
b) readout calculations
c) spectral responses

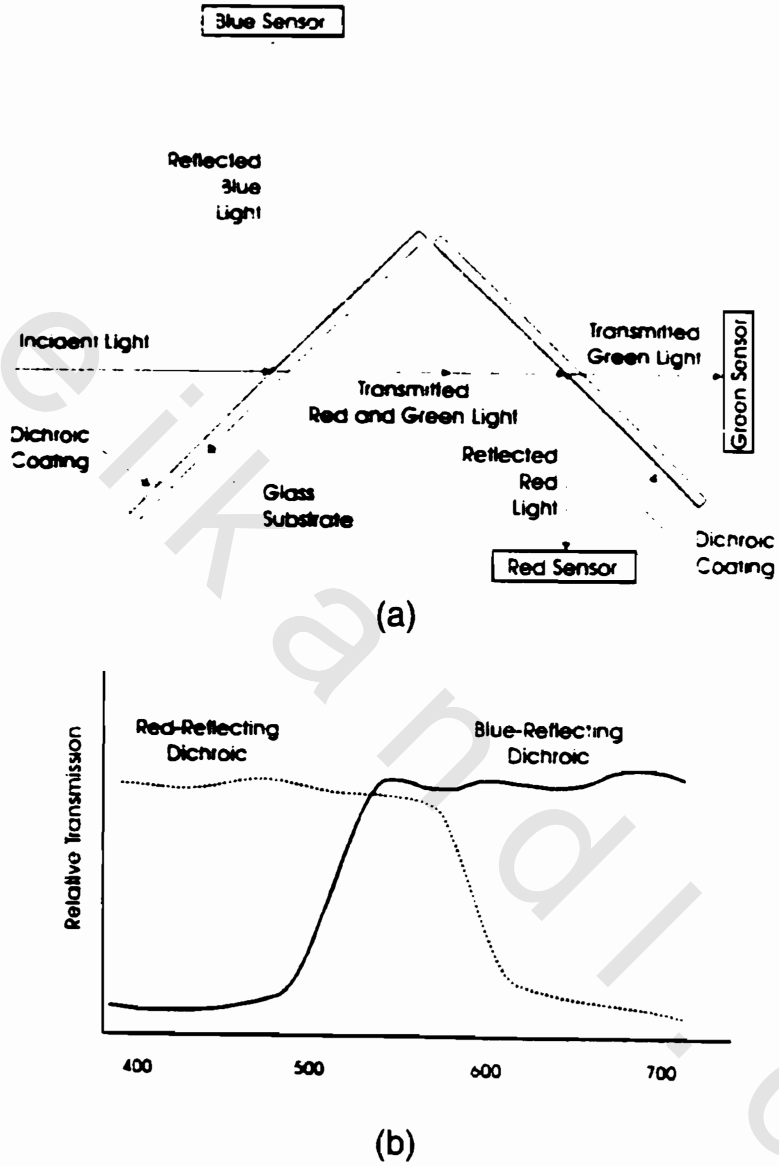


Fig 15.17 Dichroic mirror light splitter
a) optical path b) spectrum

Blue light is reflected by the first mirror, but longer wavelength passes through to the second mirror. That mirror is designed to reflect red light, but green light passes through. Thus, light is split into three components. There are a number of problems with mirror light splitting. The optical path is long, the mirror surface is affected by atmospherics, and the alignment is difficult and impractical.

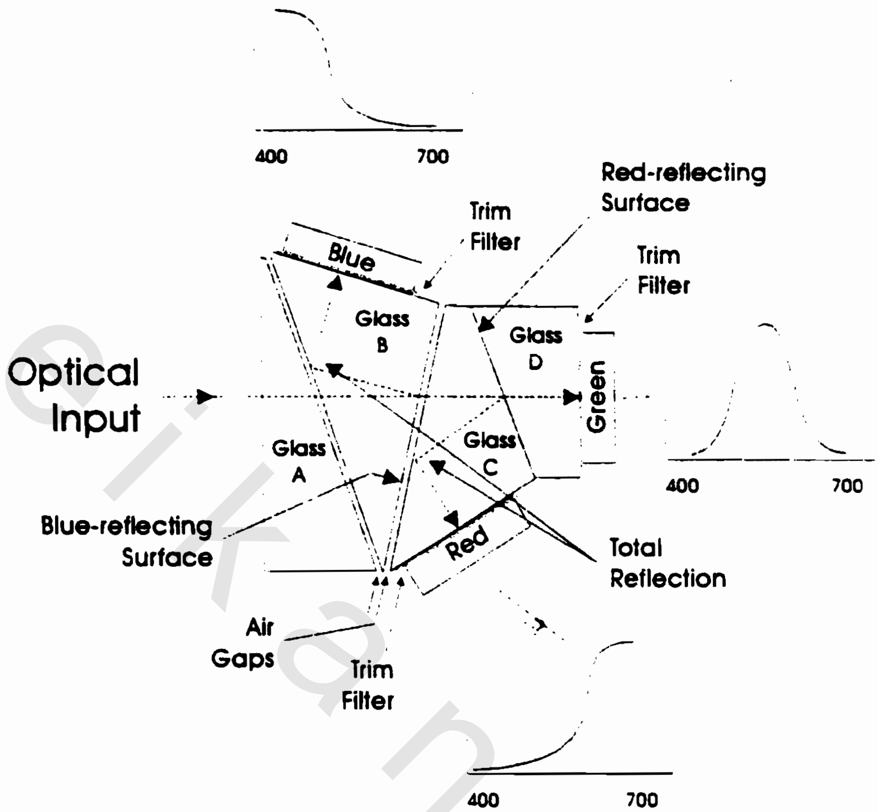


Fig. 15.18 Prism light splitter for color CCD camera

All these problems are solved with prism optics (Fig. 15.18). The dichroic coatings are placed on the surface of several solid glass prisms, which are permanently cemented together along with the imagers. This creates a reliable assembly with a minimum optical path length. Three glass prisms A, B, C are separated by air gaps. A fourth prism D is cemented to prism C. Prisms B, C, D carry the three imagers on their outer surfaces. Trim filters are placed between the imagers and prism surfaces for cutting off long wavelengths. Prisms B, C have blue reflecting and red reflecting dichroic coatings, respectively, on their surfaces farthest from the optical input. Green light passes straight through the prism assembly to the green imager. The purpose of the air gaps in the assembly is to cause total reflection of the blue and red light inside their prisms.

Prism A is added to the structure to shift the angles of light passage to avoid nontotal reflection. It also protects the dichroic coating on prism B. The prism structure ensures equal optical path for each of the imagers.

Problems:

1- Draw the complete timing diagram for Fig. 15.7.
2- Draw the complete timing diagram for Fig. 15.8.
3- Draw the timing diagram of a two-phase CCD, where charge is initially under electrode 2 for
   a) $t = t_1$, $V_1 = 0$, $V_2 = V$ b) $t = t_2$, $V_1 = 1/2$ V, $V_2 = 1/2$ V
   c) $t = t_3$, $V_1 = 3/4$ V, $V_2 = 1/4$ V   d) $t = t_4$, $V_1 = V$, $V_2 = 0$
4- A 400 by 600 pixel frame transfer CCD image sensing chip is used for 15 ms exposure time and 10 MHz readout frequency. It has 5x10 micron pixels and a pixel well capacity of 25000 electrons. The chip has readout noise of 100 electrons per pixels at an 8MHz readout rate, and 200 electrons per pixel at 20 MHz. Assume a linear relation. Find
   a) the charge storage density   b) the dynamic range
5- In the problem above, the chip has a quantum efficiency of 0.3 and dark current of 5000 electrons/second/pixel at 25°C. Assume that the incident light flux is 2 x 10^6 photons/ second/pixel. Find
   a) the dark current as a function of temperature.
   b) percent of capacity of well filling during the exposure time.
6- In the problem above, find
   a) the exposure time needed to saturate the well.
   b) S/N at 25°C.   c) photon noise level.   d) total noise level.
7- A certain 1200 by 1000 pixel full frame CCD image sensing chip has 6x6 micron pixels, and a pixel well capacity of 50000 electrons. The chip has readout noise of 5 electrons per pixel at 40 MHz readout rate and 15 electrons per pixel at 400 MHz. For a dynamic range of 5000, find the readout frequency.
8- In the problem above, the chip has a quantum efficiency of 0.5 and dark current of 0.03 electrons/second/pixel at -30°C. Find the dark current at 25°C.
9- For incident light flux of 3000 photons per second per pixel in the problem above, find the exposure time needed to saturate the wells, and then calculate the exposure time for S/N = 200 at 400 MHz readout rate. How much are the wells filled at this exposure time.
10- In the problem above, discuss the case when S/N = 100 at 400 MHz, What do you conclude?
11- Compare the different noise components in the CCD of the previous problem. Make any reasonable assumptions. What do you conclude?
12- Verify the color CCD read out procedure (Fig. 15.16b). Discuss its advantages and disadvantages.

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